INTEGRATED CIRCUITS

Semiconductors for Radio, Audio and CD/DVD Systems

1998

Data Handbook IC01
CD-ROM included

Let's make things better.

Philips
Semiconductors

PHILIPS

QUALITY ASSURED

Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programmes; and we promote a partnering relationship with our customers and suppliers.

PRODUCT SAFETY

In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility towards the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical', 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

Semiconductors for Radio, Audio and CD/DVD Systems

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Short-form specification	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

PREFACE

The audio/video market is characterized by a continuing demand for innovation to increase the functionality of ICs by achieving ever higher levels of integration, reducing power consumption, minimizing the number of peripheral components and reducing the need for circuit alignment during assembly. We achieve these goals by extensive use of computer control via the I^2C-bus, and by designing analog, digital and mixed signal circuits using the very latest signal processing techniques. We then fabricate the ICs with state-of-the-art production processes so we can offer you complete `systems-on-silicon' which help you maintain your competitive edge by staying one step ahead of the competition.

An innovative and reliable supplier

A total systems approach, embracing both hardware and software, is the foundation on which we have built our unrivalled reputation as an innovative and reliable supplier of high quality semiconductors for the audio/video segments of the consumer electronics market.

Our strengths in this field stem not only from being a large multinational organization with the resources to stay the course, but also from our dedication to research and to forming true and lasting partnerships with our customers.

World-class manufacturing, resources and customer support

Philips Semiconductors is a global supplier. We employ some 20,000 people, have more than 100 sales offices worldwide, are represented in 44 countries, and manufacture over 14,000 different products. Philips also has a level of commitment to research matched by very few companies, not just in terms of resources but in their focus on researching solutions for customers. Philips Semiconductors collaborates very closely with Philips Corporate Research Laboratories, one of the largest privately funded research organisations in the world. Five major research laboratories serve the whole group, in the Netherlands, UK, France, Germany and the USA.

As you would expect from a worldwide organization, our support doesn't end with the timely delivery of ICs and discretes to our audio/video customers. We are also dedicated to the aim of zero-defects quality for our semiconductors, and to offering unequalled service. There are Philips customer support and application centres in every major market area (Europe, Asia-Pacific, North America) to ensure that you can take full advantage of our extensive applications know-how and broad product range. Five System Laboratories are involved in programs and activities relevant to audio/video: Eindhoven, the Netherlands (TV, monitors and radio/audio); Hamburg, Germany (TV and radio/audio); Southampton, UK (teletext and digital audio, including CD technology); Taipeh, Taiwan (TV, monitors and radio/audio).

They support all audio/video applications and work closely with customers, meeting and often anticipating their needs.

Many key developments have come from Philips laboratories - one-chip TV signal processors, ICs for memory-based TV features, a TV microcontroller with on-chip teletext, a two-chip receiver module for car radio, and a one-chip self-tuned radio are just a few examples. In addition, there are also Product Development groups in all the above locations.

Partnership

Since the spur for many of the ICs and discrete semiconductors in this databook have come from a cross-fertilisation of ideas with customers, we are fully aware that we need to be not only semiconductor suppliers, but also partners who are willing to work with customers to find solutions and help keep them at the leading edge of their field. At Philips Semiconductors, we work very closely with our audio/video customers and are determined to maintain a reputation for being the world's most customer-oriented supplier.

WHAT THIS BOOK AND CD-ROM CONTAIN

This book contains

- a general section

- abstract data sheets of our most recent products,

- the alphanumeric and functional indices of all data sheets residing on the accompanying CD-ROM.

The data sheet files on the CD-ROM are in Adobe's Portable Document Format (PDF) - a cross-platform file format that requires Acrobat Reader to view (we have also supplied Acrobat Reader on the CD-ROM). Acrobat Reader enables you to view and print pages, and perform basic searches. Please refer to the README.1st file on the CD-ROM to find information on the CD's contents and organization, as well as instructions on how to install and use Acrobat Reader.

FOR MORE INFORMATION

Although the information in this databook is up-to-date at the time of going to press, the world of audio/video is so fast moving it is possible that some very recent developments may not have made it into this edition. For the latest information contact your local Philips organization (see the back page of this databook for addresses), or visit our Internet home page at: http://www.semiconductors.philips.com

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Semiconductors for Radio, Audio and CD/DVD Systems

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SELECTION GUIDES

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	TDA7053	2 x 1 W BTL portable/Mains-fed stereo power amplifier	
	TDA7053A	Stereo BTL audio output amplifiers with DC volume control	
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	TDA7056A	3 W BTL mono audio output amplifier with DC volume control	
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DISPLAY DRIVERS

LCD display

PCF1303T	18-element bar graph LCD driver	
PCF2113x	LCD controller/driver	
PCF2116 family (PCF2114X; PCF2116X)	LCD controller/drivers	
PCF8558	Universal LCD driver for small graphic panels	
PCF8566	Universal LCD driver for low multiplex rates	
PCF8576C	Universal LCD driver for low multiplex rates	
PCF8577C	LCD direct/duplex driver with I^2C-bus interface	
PCF8578	LCD row/column driver for dot matrix graphic displays	
PCF8579	LCD column driver for dot matrix graphic displays	
PCF21XXC family	LCD drivers	

LED DISPLAY

SAA1064	4-digit LED driver with I2C-bus interface	

IR REMOTE CONTROL CIRCUITS

PCA84C122; 222; 422; 622; 822	8-bit microcontrollers for remote control transmitters	
SAA3010	Infrared remote control transmitter RC-5	

REPLACEMENT / WITHDRAWAL TYPES

The following type numbers were in the previous issue of this data handbook/CD-ROM, but not in the current version.

TYPE NUMBER	REASON FOR DELETION
83CE654	Discontinued, replaced by C654 type
BB112	Discontinued
BB130	Discontinued
BB204B; BB204G	Discontinued
BB212	Discontinued
BF246A to C; BF247A to C	Discontinued
BF851A; BF851B; BF851C	Discontinued
J308/309/310	Discontinued
P8xCE528	Discontinued, replaced by C528 type
PCF8568	Discontinued
PCF8569	Discontinued, replaced by PCF8579
SAA2002	Discontinued
SAA2003	Discontinued
SAA2012	Discontinued
SAA2013	Discontinued
SAA2022	Discontinued
SAA2023	Discontinued
SAA2032	Discontinued
SAA3323	Discontinued
TDA1318	Discontinued
TDA1319T	Discontinued
TDA1380	Discontinued
TDA1381	Discontinued
TDA1383	Discontinued
TDA1546T	Discontinued
OM5604; OM5606	Discontinued, replaced by OM5610
OM5608	Discontinued
SAA1057	Discontinued
TDA1001B; TDA1001BT	Discontinued
TDA1011	Discontinued, replaced by TDA1015
TDA1015T	Discontinued, replaced by TDA1015
TDA1303	Removed from handbook
TDA1510AQ	Discontinued, replaced by TDA1515BQ
TDA1541A	Removed from handbook
TDA1602A	Discontinued
TEA0655	Discontinued
TEA0665; TEA0665T	Discontinued
TEA6310T	Discontinued

Internet World Wide Web Home Page

WHAT IS IT?

Welcome to our place in cyberspace.

Explore our Web pages and take a look at our product offering of advance High-performance Applications and Products.

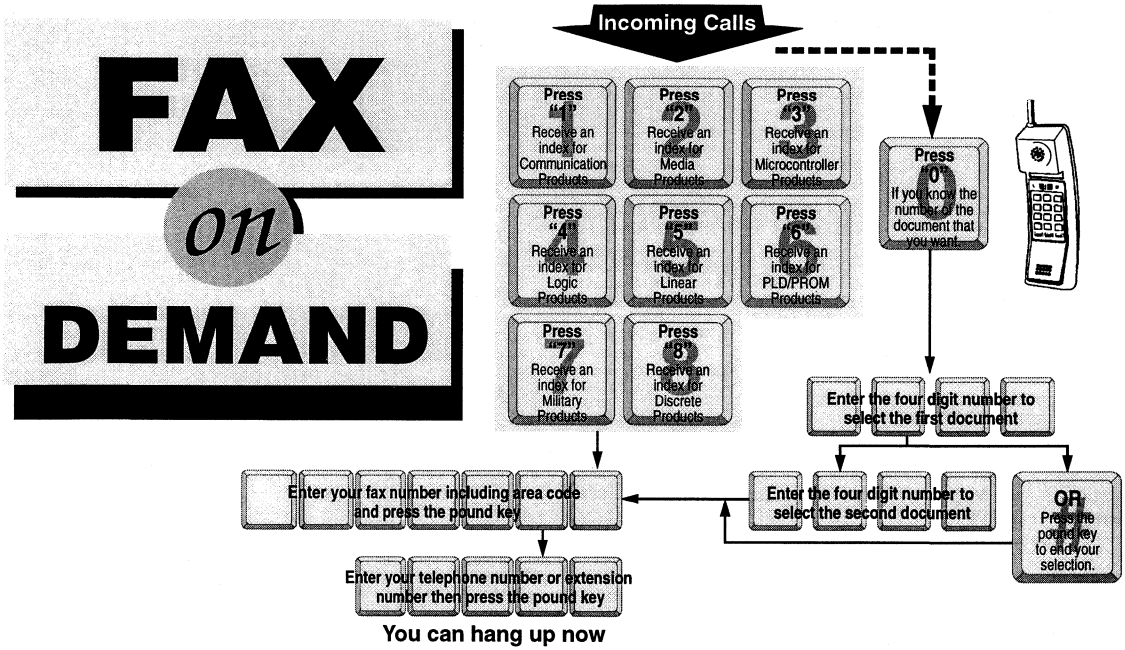
In addition, we offer you the latest information on Products, News, Support, Employment and Offices.

HOW TO REACH US

For access to the Philips Semiconductors Home Page go to the World Wide Web location:

http://www.semiconductors.philips.com/

Fax on Demand



What is it?

The FAX-on-DEMAND system is a computer facsimile system that allows customers to receive selected documents by fax automatically.

How does it work?

To order a document, you simply enter the document number. This number can be obtained by asking for an index of available documents to be faxed to you the first time you call the system.

Our system has a selection of the latest product data sheets from Philips with varying page counts. As you know, it takes approximately one minute to FAX one page. This isn't bad if the number of pages is less than 10. But if the document is 37 pages long, be ready for a long transmission!

Philips Semiconductors also maintains product information on the World-Wide Web. Our home page can be located at:
http://www.semiconductors.philips.com

Who do I contact if I have a question about FAX-on-DEMAND?

Contact your local Philips sales office.

FAX-on-DEMAND phone numbers:

England (United Kingdom, Ireland)	44-181-730-5020
France	33-1-40-99-60-60
Italy	39-167-295502
North America	1-800-282-2000

Locations soon to be in operation:

Hong Kong
Japan
The Netherlands

GENERAL

TOTAL QUALITY MANAGEMENT

Philips Semiconductors is a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is described in the following paragraphs.

Quality assurance

Based on ISO 9000 standards, customer standards such as Ford TQE and IBM MDQ. Our factories are certified to ISO 9000 by external inspectorates.

Partnerships with customers

PPM co-operations, design-in agreements, ship-to-stock, just-in-time and self-qualification programmes, and application support.

Partnerships with suppliers

Ship-to-stock, statistical process control and ISO 9000 audits.

Quality improvement programme

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

ADVANCED QUALITY PLANNING

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

PRODUCT CONFORMANCE

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- Incoming material management through partnerships with suppliers.
- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control.
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications.
- Periodic inspections to monitor and measure the conformance of products.

PRODUCT RELIABILITY

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the products reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

CUSTOMER RESPONSES

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

RECOGNITION

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organizations.

DISCRETE SEMICONDUCTORS

Basic type number

This type designation code applies to discrete semiconductor devices (not integrated circuits), multiples of such devices, semiconductor chips and Darlington transistors.

FIRST LETTER

The first letter gives information about the material for the active part of the device.

A Germanium or other material with a band gap of 0.6 to 1 eV

B Silicon or other material with a band gap of 1 to 1.3 eV

C Gallium arsenide (GaAs) or other material with a band gap of 1.3 eV or more

R Compound materials, e.g. cadmium sulphide.

SECOND LETTER

The second letter indicates the function for which the device is primarily designed. The same letter can be used for multi-chip devices with similar elements.

In the following list low power types are defined by $R_{th\ j\text{-}mb} > 15$ K/W and power types by $R_{th\ j\text{-}mb} \leq 15$ K/W.

A Diode; signal, low power

B Diode; variable capacitance

C Transistor; low power, audio frequency

D Transistor; power, audio frequency

E Diode; tunnel

F Transistor; low power, high frequency

G multiple of dissimilar devices/miscellaneous devices; e.g. oscillators. Also with special third letter, see under "Serial number/special third letter"

H Diode; magnetic sensitive

L Transistor; power, high frequency

N Photocoupler

P Radiation detector; e.g. high sensitivity photo-transistor; with special third letter

Q Radiation generator; e.g. LED, laser; with special third letter

R Control or switching device; e.g. thyristor, low power; with special third letter

S Transistor; low power, switching

T Control and switching device; e.g. thyristor, power; with special third letter

U Transistor; power, switching

W Surface acoustic wave device

X Diode; multiplier, e.g. varactor, step recovery

Y Diode; rectifying, booster

Z Diode; voltage reference or regulator, transient suppressor diode; with special third letter.

SERIAL NUMBER/SPECIAL THIRD LETTER

The number comprises three figures running from 100 to 999 for devices primarily intended for consumer equipment, or one letter (Z, Y, X, etc.) and two figures running from 10 to 99 for devices primarily intended for industrial or professional equipment.(1) The letter has no fixed meaning, except in the following cases:

A For triacs, after second letter 'R' or 'T'

F For emitters and receivers in fibre-optic communication, after second letter 'G', 'P' or 'Q'. When the second letter is 'G', the first letter should be defined in accordance with the material of the main optical device.

L For lasers in non-fibre-optic applications, after second letter 'G' or 'Q'. When the second letter is 'G', the first letter should be defined in accordance with the material of the main optical device.

O For opto-triacs, after second letter 'R'

T For 3-state bicolour LEDs, after second letter 'Q'

W For transient voltage suppressor diodes, after second letter 'Z'.

EXAMPLES OF BASIC TYPE NUMBERS

AA112 Germanium, low power signal diode (consumer type)

ACY32 Germanium, low power AF transistor (industrial type)

BD232 Silicon, power AF transistor (consumer type)

CQY17 GaAs, light-emitting diode (industrial type)

RPY84 CdS, photo-conductive cell (industrial type).

Version letter(s)

One or two letters may be added to the basic type number to indicate minor electrical or mechanical variants of the basic type. The letters never have a fixed meaning, except that the letter 'R' indicates reverse polarity and the letter 'W' indicates a surface mounted device (SMD).

(1) When the supply of these serial numbers is exhausted, the serial number may be expanded to three figures for industrial types and four figures for consumer types.

Suffix

Sub-classification can be used for devices supplied in a wide range of variants, called associated types. The following sub-coding suffixes are in use:

VOLTAGE REFERENCE AND VOLTAGE REGULATOR DIODES

One letter and one number, preceded by a hyphen (-). The letter, if required, indicates the nominal tolerance of the Zener voltage.

A 1%

B 2%

C 5%

D 10%

E 20%.

In the case of a 3% tolerance, the letter 'F' is used.

The number denotes the typical operating (Zener) voltage, related to the nominal current rating for the entire range. The letter 'V' is used in place of the decimal point.

Example: BZY74-C6V3 or -C10.

TRANSIENT VOLTAGE SUPPRESSOR DIODES

One number, preceded by a hyphen (-). The number indicates the maximum recommended continuous reversed (stand-off) voltage, V_R. The letter 'V' is used in place of the decimal point.

Example: BZW70-9V1 or –39.

The letter 'B' may be used immediately after the last number, to indicate a bidirectional suppressor diode.

Example: BZW10-15B.

CONVENTIONAL AND CONTROLLED AVALANCHE RECTIFIER DIODES AND THYRISTORS

One number, preceded by a hyphen (-). The number indicates the rated maximum repetitive peak reverse voltage, V_{RRM}, or the rated repetitive peak off-state voltage, V_{DRM}, whichever is the lower. Reversed polarity with respect to the case is indicated by the letter 'R' immediately after the number.

Example: BYT-100 or -100R.

RADIATION DETECTORS

One number, preceded by a hyphen (-). The number indicates the depletion layer in micrometres (μm). The resolution is indicated by a version letter.

Example: BPX10-2A.

ARRAY OF RADIATION DETECTORS AND GENERATORS

One number, preceded by a hyphen (-). The number indicates the number of basic devices assembled into the array.

Examples: BPW50-6, BPW50-9, BPW50-12.

HIGH FREQUENCY POWER TRANSISTORS

One number, preceded by a hyphen (-). The number indicates the supply voltage.

Example: BLU80-24.

INTEGRATED CIRCUITS

Basic type number

This type designation code applies to semiconductor monolithic, semiconductor multi-chip, thin film, thick film and hybrid integrated circuits. The basic type number comprises three letters followed by a serial number.

FIRST AND SECOND LETTERS

Digital family circuits

The first two letters identify the family.(1)

Solitary circuits

The first letter divides solitary circuits into:

S Solitary digital circuits

T Analog circuits

U Mixed analog/digital circuits.

The second letter is a serial letter without any further significance except 'H' which stands for hybrid circuits.(2)

Microprocessors

The first two letters identify microprocessors and related circuits:

MA Microcomputer or central processing unit

MB Slice processor (functional slice of microprocessor)

(1) A logic family is an assembly of digital circuits designed to be interconnected and defined by its base electrical characteristics, such as supply voltage, power consumption, propagation delay, noise immunity.

(2) The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added, for example, SH for bubble memories.

MD Related memories

ME Other related circuits such as interfaces, clocks, peripheral controllers, etc.

Charge-transfer devices and switched capacitors

The first two letters identify:

MH Hybrid circuits

ML Logic circuits

MM Memories

MS Analog signal processing using switched capacitors

MT Analog signal processing using charge-transfer devices

MX Imaging devices

MY Other related circuits.

THIRD LETTER

The third letter indicates the operating ambient temperature range:

A temperature range not specified below

B 0 to + 70 °C

C −55 to +125 °C

D −25 to + 70 °C

E −25 to + 85 °C

F −40 to + 85 °C

G −55 to + 85 °C.

If a device has another temperature range, the letter 'A' or a letter indicating a narrower temperature may be used, for example, the range of 0 to +75 °C can be indicated by 'A' or 'B'. Should two devices with the same basic type number both have temperature ranges other than those specified, one would use the letter 'A' and the other the letter 'X'.

Serial number

This may be a four-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

Version letter

A single version letter may be added to the basic type number. This indicates a minor variant of the basic type or the package. The version letter has no fixed meaning except for 'Z' which means customized wiring. The following letters are recommended for package variants:

C Cylindrical

D Ceramic dual in-line (CERDIL, CERDIP)

F Flat pack (two leads)

G Flat pack (four leads)

H Quad flat pack (QFP)

L Chip on tape (foil)

P Plastic dual in-line (DIL)

Q Quad in-line (QUIL)

T Mini pack (SOL, SO, VSO)

U Uncased chip.

Two-letter suffix

A two-letter suffix may be used instead of a single package version letter to give more information. To avoid confusion with serial numbers that end with a letter, a hyphen should precede the suffix.

FIRST LETTER (GENERAL SHAPE)

C Cylindrical

D Dual in-line (DIL)

E Power DIL (with external heatsink)

F Flat pack (leads on two sides)

G Flat pack (leads on four sides)

H Quad flat pack (QFP)

K Diamond (TO-3 family)

M Multiple in-line (except dual, triple and quad)

Q Quad in-line (QUIL)

R Power QUIL (with external heatsink)

S Single in-line (SIL)

T Triple in-line

W Leaded chip carrier (LCC)

X Leadless chip carrier (LLCC)

Y Pin grid array (PGA).

SECOND LETTER (MATERIAL)

C Metal-ceramic

G Glass-ceramic

M Metal

P Plastic.

Examples

PCF1105WP: digital IC; PC family; operating temperature range –40 to +85 °C; serial number 1105; plastic leaded chip carrier.

GMB74LS00A-DC: digital IC; GM family; operating temperature range 0 to +70 °C; company number 74LS00A; ceramic DIL package.

TDA1000P: analog IC; operating temperature range non-standard; serial number 1000; plastic DIL package.

SAC2000: solitary digital circuit; operating temperature range –55 to +125 °C; serial number 2000.

RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

ELECTROSTATIC CHARGES

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our MOS devices are internally protected against electrostatic discharge but they **can** be damaged if the following precautions are not taken.

WORK STATION

Figure 1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ per cm^2. The floor should also be covered with antistatic material. The following precautions should be observed:

- Persons at a work bench should be earthed via a wrist strap and a resistor.
- All mains-powered electrical equipment should be connected via an earth leakage switch.
- Equipment cases should be earthed.
- Relative humidity should be maintained between 50 and 65%.
- An ionizer should be used to neutralize objects with immobile static charges.

RECEIPT AND STORAGE

MOS devices are packed for dispatch in antistatic/conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any MOS devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

ASSEMBLY

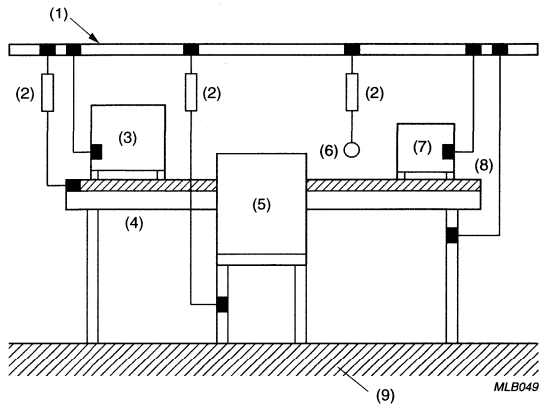
MOS devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the MOS devices are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards containing MOS devices should be handled in the same way as unmounted MOS devices. They should also carry warning labels and be packed in conductive or antistatic packing.



(1) Earthing rail.
(2) Resistor (500 kΩ ± 10%, 0.5 W).
(3) Ionizer.
(4) Work bench.
(5) Chair.
(6) Wrist strap.
(7) Electrical equipment.
(8) Conductive surface/antistatic sheet.
(9) Antistatic floor.

Fig.1 Protected work station.

DEVICE DATA

Matchbox global FM tuner OM5610

FEATURES

- Local/DX switching to improve large signal handling on FM when an outdoor antenna or cable network is connected
- MPX-RDS signal available
- The module meets the *"FCC regulations"*
- Small size.

ORDERING INFORMATION

UNIT	FREQUENCY (MHz)	BUS
OM5610	87.5 to 108	3-wire bus

GENERAL DESCRIPTION

The OM5610 is a global FM-radio tuner (except Japan) which includes a brand new concept in tuning techniques. The new tuning concept combines the advantages of hand tuning together with electronic facilities and features.

TOP VIEW

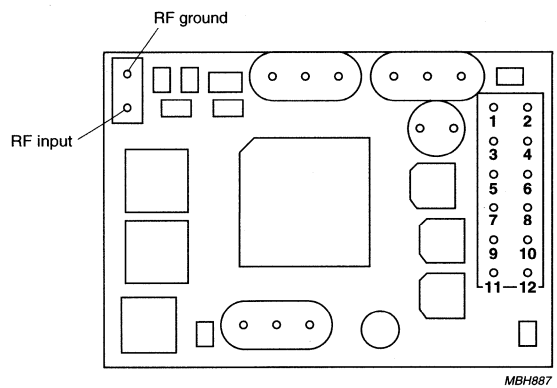


Fig.1 OM5610 connectors.

PINNING

PIN	DESCRIPTION
1	ground
2	ground
3	WREN
4	CLCK
5	STEREO
6	DATA
7	supply voltage (+5 V)
8	supply voltage (+12 V)
9	audio right output
10	ground
11	audio left output
12	MPX-RDS

CONTENTS

1 FEATURES

- Low sampling frequency decoding possibilities (24 kHz, 22.05 kHz and 16 kHz) of MPEG2 are supported
- A variety of output formats are supported: I^2S, SPDIF and 256 or more times oversampled bit serial analog stereo
- Automatic internal dynamic range compression algorithm using programmable compression parameters
- Non byte-aligned coded input data is handled
- Built-in provisions to generate high quality sampling clocks for all six supported sampling frequencies; these sampling clocks may locked to an external PLL to support an extensive list of input data reference clock frequencies
- Bit-rate and sampling-rate settings may be overruled by the microcontroller while the SAA2502 is trying to establish frame synchronization
- Input interface mode which requests data based on input buffer content, enables the handling of variable bit-rate input streams and input data offered in (fixed length) bursts
- An interrupt output pin which can generate interrupt requests at the occurrence of various events; consequently polling by the microcontroller is not needed in most situations
- L3 and the I^2C-bus microcontroller interface protocols are supported
- The control interface is always fully operational (also while STOP is asserted)
- CRC protection of scale factors is provided for all supported sample frequencies.

2 APPLICATIONS

- Astra Digital Radio (ADR)
- Digital Audio Broadcast (DAB)
- Digital Versatile Disc (DVD)
- Digital Video Broadcast (DVB)
- General purpose MPEG2 audio decoding.

3 GENERAL DESCRIPTION

The SAA2502 is a second generation ISO/MPEG audio source decoder. The device specification has been enhanced with respect to the SAA2500 and SAA2501 ICs and therefore it offers in principle all features of its predecessors.

It supports layer I and II of MPEG1 and the MPEG2 requirements for a stereo decoder.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA2502H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

5 BLOCK DIAGRAM

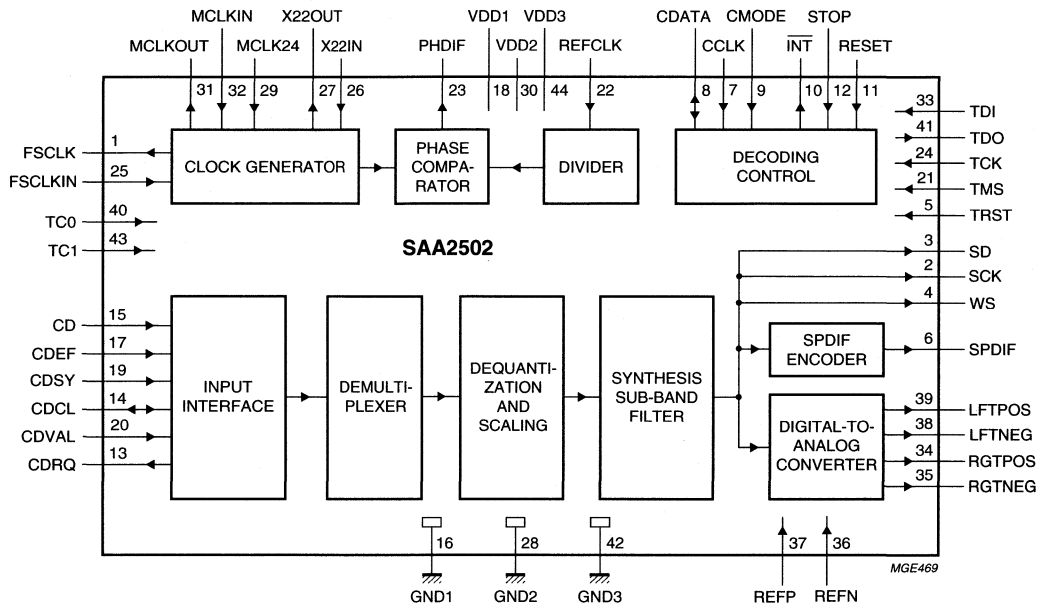


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
FSCLK	1	sample rate clock output; buffered signal
SCK	2	baseband audio data I^2S clock output
SD	3	baseband audio I^2S data output
WS	4	baseband audio data I^2S word select output
TRST	5	boundary scan test reset input
SPDIF	6	SPDIF baseband audio output
CCLK	7	L3 clock/I^2C-bus bit clock input
CDATA	8	L3 data/I^2C-bus serial data input/output; note 1
CMODE	9	L3 mode (address/data select input)
$\overline{INT}$	10	interrupt request output; active LOW; note 1
RESET	11	master reset input
STOP	12	soft reset/stop decoding input
CDRQ	13	coded data request output
CDCL	14	coded data bit clock input/output; note 2
CD	15	MPEG coded data input
GND1	16	ground 1
CDEF	17	coded data error flag input
V_{DD1}	18	supply voltage 1
CDSY	19	coded data byte or frame sync input
CDVAL	20	coded data valid flag input
TMS	21	boundary scan test mode select input
REFCLK	22	PLL reference clock input
PHDIF	23	PLL phase comparator output; note 2
TCK	24	boundary scan test clock input
FSCLKIN	25	sample rate clock input
X22IN	26	22.579 MHz clock oscillator input or signal input
X22OUT	27	22.579 MHz clock oscillator output
GND2	28	ground 2
MCLK24	29	master clock frequency indication input
V_{DD2}	30	supply voltage 2
MCLKOUT	31	master clock oscillator output
MCLKIN	32	master clock oscillator input or signal input
TDI	33	boundary scan test data input
RGTPOS	34	analog right channel positive output
RGTNEG	35	analog right channel negative output
REFN	36	low reference voltage input for analog outputs
REFP	37	high reference voltage input for analog outputs
LFTNEG	38	analog left channel negative output
LFTPOS	39	analog left channel positive output
TC0	40	factory test scan chain control 0 input

SYMBOL	PIN	DESCRIPTION
TDO	41	boundary scan test data output
GND3	42	ground 3
TC1	43	factory test scan chain control 1 input
V_{DD3}	44	supply voltage 3

Notes

1. Output type is: open-drain.
2. Output type is: 3-state.

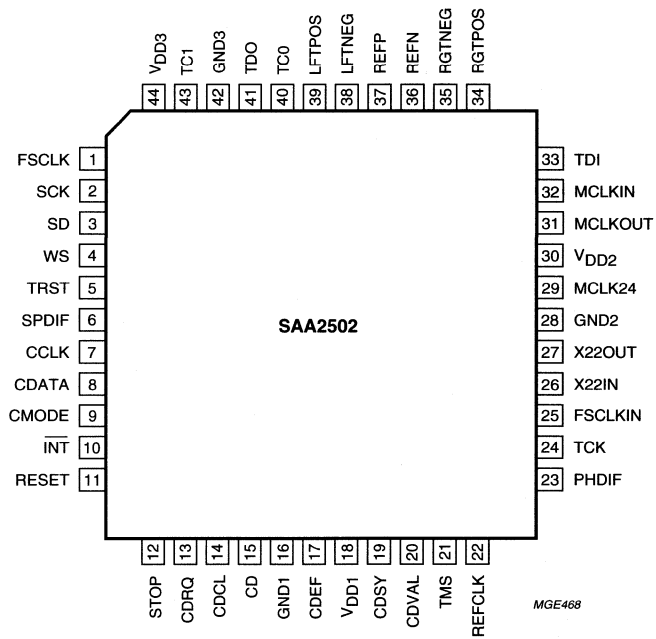


Fig.2 Pin configuration.

Video CD (VCD) decoder SAA2510

FEATURES

(With standard microcode loaded)

- Decoding and display of MPEG1 video streams (constrained parameters)
- Decoding of MPEG audio streams (layer II)
- Decoding, storage (compressed) and display of high-resolution still pictures of 704 × 576 pixels
- Requires only 4 Mbits of external 70 ns DRAM
- Audio transparency mode for CD-DA discs
- On-screen display capability
- Play options:
  - Play
  - Stop
  - Pause/continue
  - Slow-motion forward
  - Scan forward
  - Scan backward.
- Supports auto-pause feature
- Disc interface: Philips I²S, EIAJ, MEC formats and IEC 958 (EBU) interface
- Separate error flag input (EFIN) and data valid input (NDAV)
- Performs basic block decoder functions:
  - serial-to-parallel conversion
  - sync detection
  - descrambling
  - EDC calculation
  - error-correction for mode 2 form 1 sectors
  - header and sub-header interpretation.
- I²C-bus interface
- Video output YUV 4 : 2 : 2 format. DMSD bus compatible
- Also supports CCIR656 video interface, including line and field timing codes
- Audio output: 44.1 kHz. 16, 18 or 20 bits per audio sample in Philips I²S, Sony or MEC formats
- EBU audio output, fully transparent from input to output in CD-DA mode and generated in MPEG mode
- Downloadable microcode for internal controllers
- Internal video timing generator
- Requires 40 MHz crystal for system clock generation
- Requires 27 MHz crystal or external 27 MHz source for video timing generation
- Requires 16.9344 MHz (384 × 44.1 kHz) clock locked to CD drive
- Internal generation of 90 kHz MPEG clock
- Capability of sharing external DRAM by 3-stating all DRAM pins.

APPLICATION

- Dedicated video CD players.

GENERAL DESCRIPTION

MPEG1 audio and video CD (VCD) decoder, intended for use in low-cost dedicated video CD players. When used with a 4 Mbit DRAM and a digital video encoder, the decoder adds the required functionality to a CD decoder to implement a low-cost video CD player capable of playing discs coded to version 2.0 of the video CD specification. The SAA2510 is an I²C-bus controlled chip and features serial data input in four common bus formats. It provides digital video output in CCIR601 and 656 formats.

A bit-mapped on-screen display is provided and output video timing can be 525 lines/30 frames per second or 625 lines/25 frames per second. The chip is microcode programmable for feature enhancement.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA2510	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.7 mm; high stand-off height	SOT317-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD3}	supply voltage	3.0	3.3	3.6	V
V_{DD5}	supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	tbf	–	mA
$f_{xtal\ s}$	system clock crystal frequency	–	40.0	–	MHz
$f_{xtal\ v}$	video clock crystal frequency	–	27.0	–	MHz
f_i	audio clock input frequency	–	16.9344	–	MHz
T_{amb}	operating ambient temperature	–20	–	+70	°C

BLOCK DIAGRAM

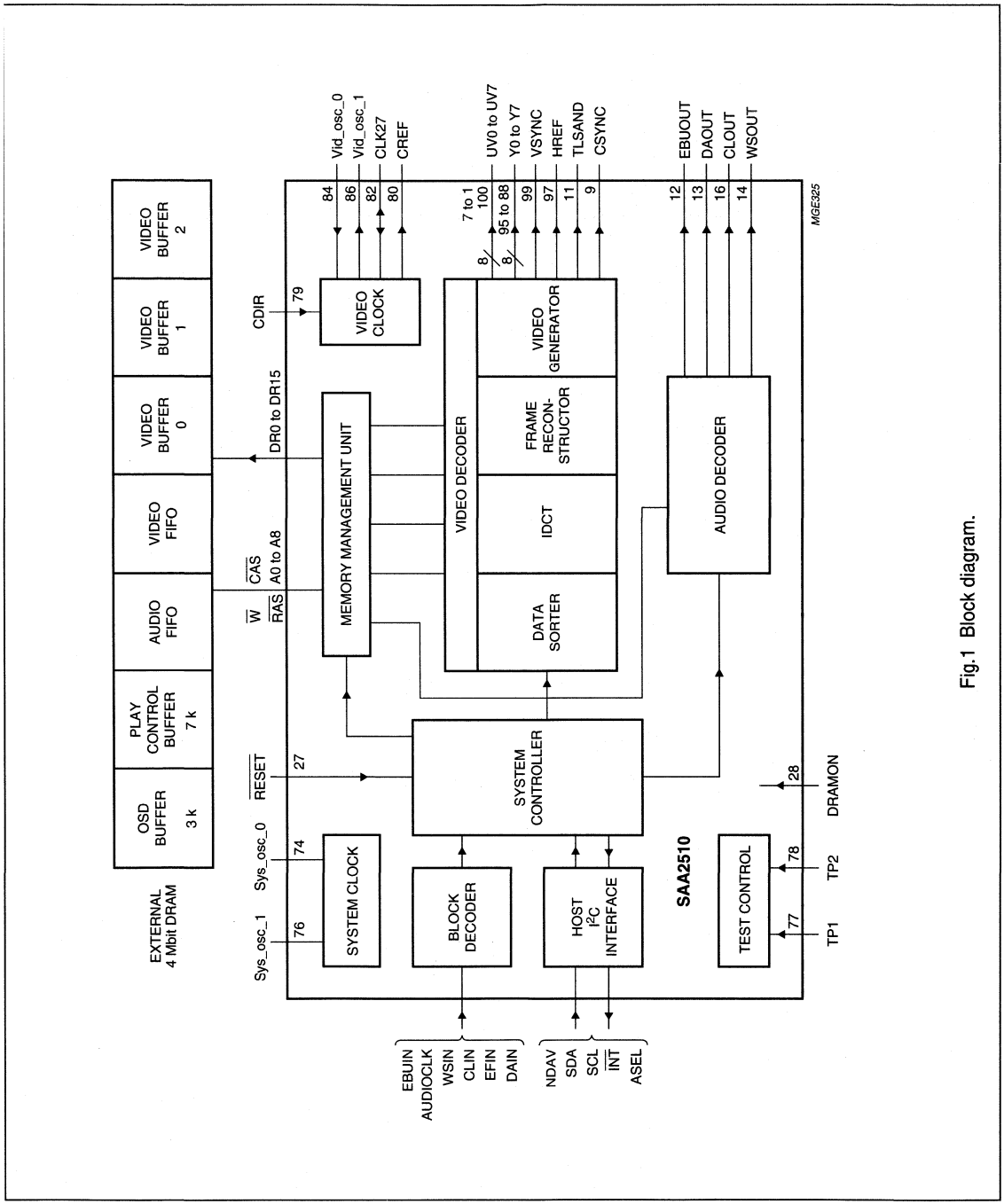


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
UV6	1	video UV bus output bit 6; 16-bit video output mode: the UV bus outputs alternating U and V chroma samples at 13.5 Mbytes/s CCIR656 mode: this bus is not used (inactive)
UV5	2	video UV bus bit 5
UV4	3	video UV bus bit 4
UV3	4	video UV bus bit 3
UV2	5	video UV bus bit 2
UV1	6	video UV bus bit 1
UV0	7	video UV bus bit 0
V_{DD5}	8	5 V external pad power supply
CSYNC	9	composite sync output; 525 lines/60 Hz or 625 lines/50 Hz
V_{SS5}	10	0 V external pad power supply
TLSAND	11	two-level Sandcastle (composite blanking) output; requires external resistor network to define horizontal/vertical blanking level
EBUOUT	12	IEC 958 digital audio output
DAOUT	13	I^2S data; digital audio output
WSOUT	14	I^2S word select digital audio output
V_{DD3}	15	+3 V internal power supply
CLOUT	16	I^2S bit clock output
V_{SS}	17	0 V internal power supply
AUDIOCLK	18	16.9 MHz audio clock input
V_{DD5}	19	5 V internal power supply
EBUIN	20	EBU (IEC 958) input
CLIN	21	I^2S bit clock input
WSIN	22	I^2S word select input
DAIN	23	I^2S digital data input
V_{DD3}	24	+3 V internal power supply
EFIN	25	error flag input from I^2S source
V_{SS}	26	0 V internal power supply
$\overline{RESET}$	27	active low reset input
DRAMON	28	DRAM pin 3-state control input; also 3-states video outputs and some timing signals
$\overline{INT}$	29	active low open drain interrupt request to host microcontroller
NDAV	30	data not valid input (data on I^2S or EBU input not valid)
ASEL	31	I^2C-bus address select pin
SDA	32	I^2C-bus data pin
V_{DD5}	33	5 V external pad power supply
SCL	34	I^2C-bus clock input
V_{SS5}	35	0 V external pad power supply
DR15	36	DRAM data input/output bit 5

SYMBOL	PIN	DESCRIPTION
DR14	37	DRAM data input/output bit 14
DR13	38	DRAM data input/output bit 13
DR12	39	DRAM data input/output bit 12
DR11	40	DRAM data input/output bit 11
DR10	41	DRAM data input/output bit 10
DR9	42	DRAM data input/output bit 9
V_{DD5}	43	5 V external pad power supply
DR8	44	DRAM data input/output bit 8
V_{SS5}	45	0 V external pad power supply
DR7	46	DRAM data input/output bit 7
DR6	47	DRAM data input/output bit 6
DR5	48	DRAM data input/output bit 5
DR4	49	DRAM data input/output bit 4
DR3	50	DRAM data input/output bit 3
DR2	51	DRAM data input/output bit 2
DR1	52	DRAM data input/output bit 1
DR0	53	DRAM data input/output bit 0
V_{SS5}	54	0 V external pad power supply
$\overline{CAS}$	55	DRAM column address strobe
V_{DD5}	56	5 V external pad power supply
A8	57	DRAM row/column address pin A8
A7	58	DRAM row/column address pin A7
A6	59	DRAM row/column address pin A6
A5	60	DRAM row/column address pin A5
A4	61	DRAM row/column address pin A4
V_{DD3}	62	+3 V internal power supply
$\overline{W}$	63	active low DRAM write strobe
V_{SS}	64	0 V internal power supply
$\overline{RAS}$	65	DRAM row address strobe
V_{DD5}	66	5 V internal power supply
A3	67	DRAM row/column address pin A3
V_{SS5}	68	0 V external pad power supply
A2	69	DRAM row/column address pin A2
V_{DD5}	70	5 V external pad power supply
A1	71	DRAM row/column address pin A1
A0	72	DRAM row/column address pin A0
V_{DDO3}	73	3 V internal power supply for oscillator
Sys_osc_0	74	oscillator input pin; 40 MHz oscillator
V_{SS}	75	0 V internal power supply
Sys_osc_1	76	oscillator output pin; 40 MHz oscillator
TP1	77	factory test pin; connect to ground

SYMBOL	PIN	DESCRIPTION
TP2	78	factory test pin; connect to ground
CDIR	79	clock direction control pin; when high, CLK27 is an output
CREF	80	clock qualifier output; 13.5 MHz timing signal used in 16-bit video output mode; can also be used as 13.5 MHz video sample clock
V_{SS5}	81	0 V external pad power supply
CLK27	82	27 MHz clock input or output; direction controlled by CDIR pin
V_{DD5}	83	5 V external pad power supply
Vid_osc_0	84	oscillator pin; 27 MHz; input pin
V_{SS}	85	0 V internal power supply
Vid_osc_1	86	oscillator pin; 27 MHz; output pin
V_{DDO3}	87	3 V internal power supply for oscillator
Y7	88	video Y bus output bit 7 DMSD mode: the Y bus outputs luminance samples at 13.5 Mbytes/s CCIR656 mode: this pin supplies multiplexed chrominance and luminance (27 Mbytes/s)
Y6	89	video Y bus bit 6
Y5	90	video Y bus bit 5
Y4	91	video Y bus bit 4
Y3	92	video Y bus bit 3
Y2	93	video Y bus bit 2
Y1	94	video Y bus bit 1
Y0	95	video Y bus bit 0
V_{SS5}	96	0 V external pad power supply
HREF	97	horizontal (line) timing reference signal; high during active video part of line, low during line blanking
V_{DD5}	98	5 V external pad power supply
VSYNC	99	vertical (field/frame) timing reference signal; high during vertical blanking interval of field
UV7	100	video UV bus output bit 7 DMSD mode: the UV bus outputs alternating U and V chroma samples at 13.5 Mbytes/s CCIR656 mode: this bus is not used (inactive)

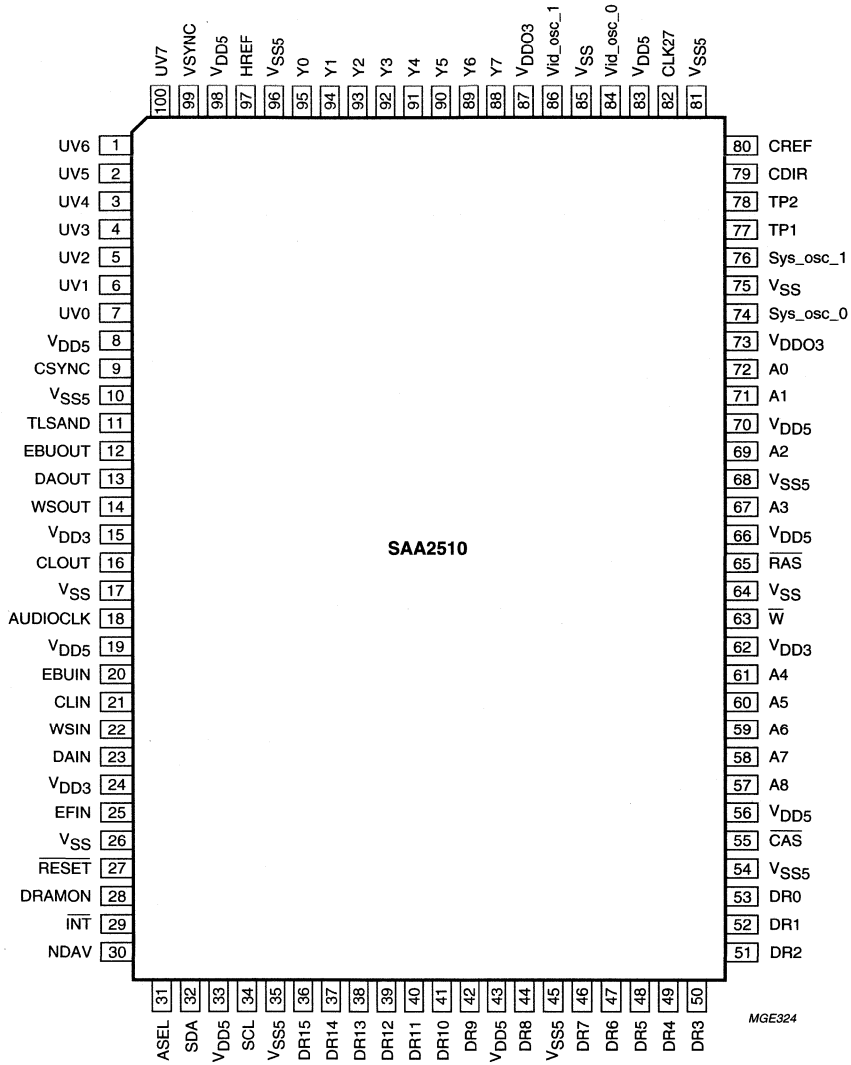


Fig.2 Pin configuration.

Stereo filter and codec for MPEG layer 1 audio applications

SAA2520

FEATURES

- Stereo filtering and codec functions in a single chip
- MPEG coded interface
- Filtered data interface
- Baseband audio data interface
- LT interface to microcontroller
- Clock generator
- Low operating voltage capability.

GENERAL DESCRIPTION

The SAA2520 performs the sub-band filtering and audio frame codec functions to provide efficient audio compression/decompression for MPEG (11172-3) Layer1 applications. It is capable of functioning as a stand-alone decoder but requires the addition of an adaptive masking threshold processor (SAA2521) in order to function as a highly efficient encoder.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA2520GP[1]	44	QFP	plastic	SOT205AG

Note

1. SOT205-1; 1996 August 26.

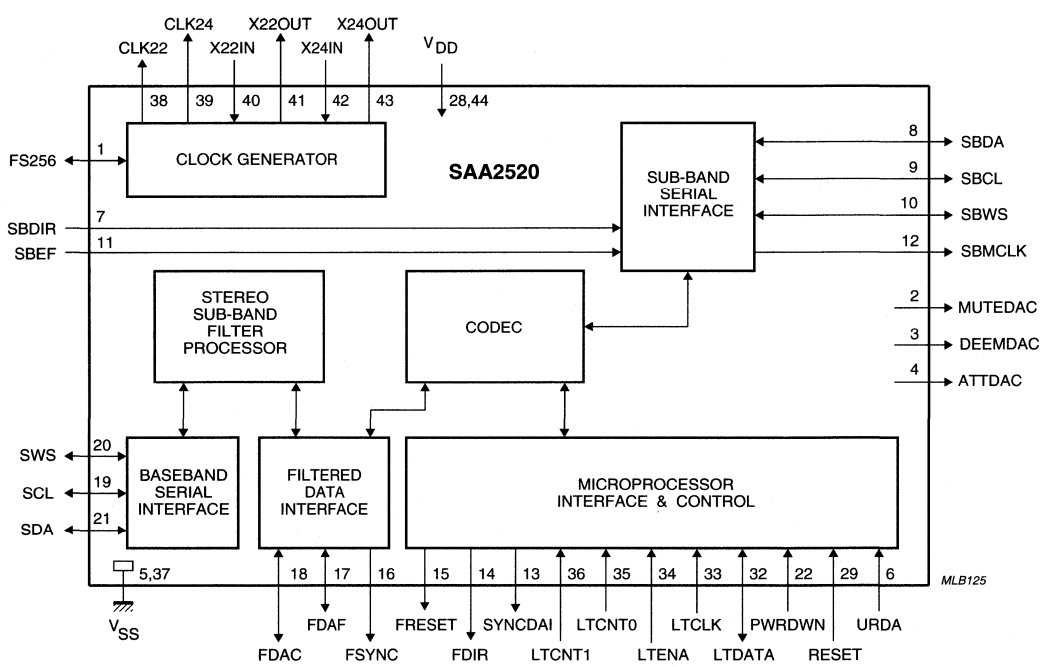


Fig.1 Block diagram.

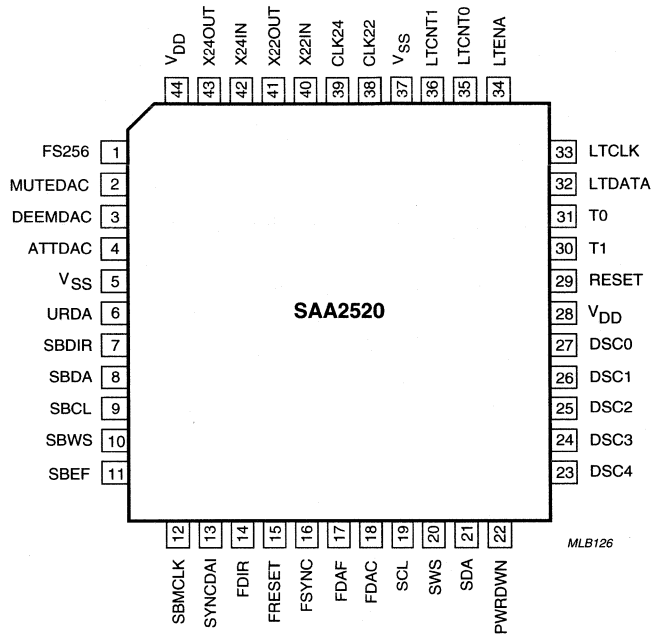


Fig.2 Pin configuration.

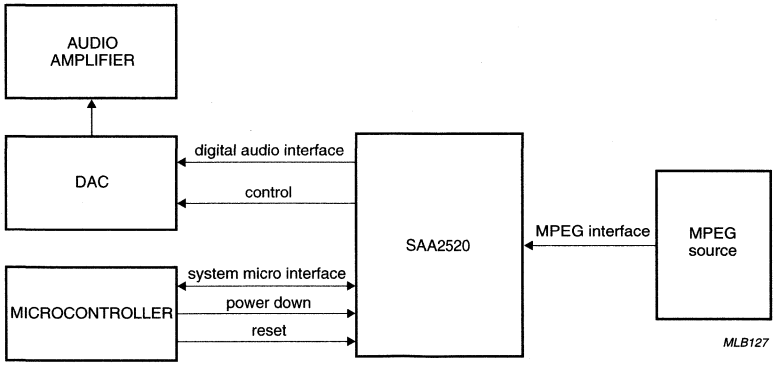


Fig.3 MPEG decoder system data flow diagram.

PINNING

SYMBOL	PIN	DESCRIPTION	TYPE
FS256	1	(Filtered)-I²S clock; 256 × sample frequency. 12 mA 3-state output + CMOS input with pull-down	I/O
MUTEDAC	2	DAC control/output expander	O
DEEMDAC	3	DAC control/output expander	O
ATTDAC	4	DAC control/output expander	O
V_{SS}	5	supply ground (0 V)	
URDA	6	unreliable drive processing data; CMOS level	I
SBDIR	7	sub-band I²S direction: (SWBS, SBCL, SBDA); CMOS level	I
SBDA	8	sub-band I²S data; 4 mA, 3-state output + CMOS input with pull-down	I/O
SBCL	9	sub-band I²S bit clock; 4 mA, 3-state output + CMOS input with pull-down	I/O
SBWS	10	sub-band I²S word select; 4 mA, 3-state output + CMOS input with pull-down	I/O
SBEF	11	sub-band I²S byte error flag; CMOS level	I
SBMCLK	12	sub-band I²S clock, 6.144 MHz locked to FS256; 8 mA, 3-state output + CMOS input with pull-down	O
SYNCDAI	13	DAI synchronization pulse	O
FDIR	14	(Filtered)-I²S direction: (FDAC, FDAF, SDA);	O
FRESET	15	reset signal for SAA2521	O
FSYNC	16	Filtered-I²S sync signal for SAA2521	O
FDAF	17	Filtered-I²S sub-band filter data; 4 mA, 3-state output + CMOS input with pull-down	I/O
FDAC	18	Filtered-I²S sub-band codec data; 4 mA, 3-state output + CMOS input with pull-down	I/O
SCL	19	I²S bit clock; 4 mA, 3-state output + CMOS input with pull-down	I/O
SWS	20	I²S-word select; 4 mA, 3-state output + CMOS input with pull-down	I/O
SDA	21	I²S baseband data filter; 4 mA, 3-state output + CMOS input with pull-down	I/O
PWRDWN	22	power-down mode; CMOS level	I
DSC4	23	test pin	
DSC3	24	test pin	
DSC2	25	test pin	
DSC1	26	test pin	
DSC0	27	test pin	
V_{DD}	28	positive supply voltage (+5 V)	
RESET	29	system reset; CMOS level with pull-down and hysteresis	I
T1	30	test pin; do not connect	
T0	31	test pin; do not connect	
LTDATA	32	LT interface data; 4 mA, 3-state output + CMOS input with pull-down	I/O
LTCLK	33	LT interface bit clock; CMOS level	I

SYMBOL	PIN	DESCRIPTION	TYPE
LTENA	34	LT interface enable; CMOS level	I
LTCNT0	35	LT interface control; CMOS level	I
LTCNT1	36	LT interface control; CMOS level	I
V_{SS}	37	supply ground (0 V)	
CLK22	38	22.5792 MHz buffered output	O
CLK24	39	24.576 MHz buffered output	O
X22IN	40	22.5792 MHz crystal input	I
X22OUT	41	22.5792 MHz crystal output	O
X24IN	42	24.576 MHZ crystal input	I
X24OUT	43	24.576 MHz crystal output	O
V_{DD}	44	positive supply voltage (+5 V)	

Masking threshold processor for MPEG layer 1 audio compression applications

SAA2521

FEATURES

- Stereo or 2-channel mono encoding
- Status may be read continuously
- Microcontroller interface
- I^2S-interfaces
- Allocation algorithm including optional emphasis correction (for 44.1 kHz)
- Reduced power consumption
- 4 V nominal operating voltage capability.

GENERAL DESCRIPTION

The SAA2521 performs the adaptive allocation and scaling function for calculating the masking thresholds and sub-band sample accuracy in MPEG layer 1 applications. The SAA2521 is intended for use in conjunction with the stereo filter codec SAA2520.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA2521GP	44	QFP	plastic	SOT205AG[1]

Note

1. SOT205-1; 1996 August 23.

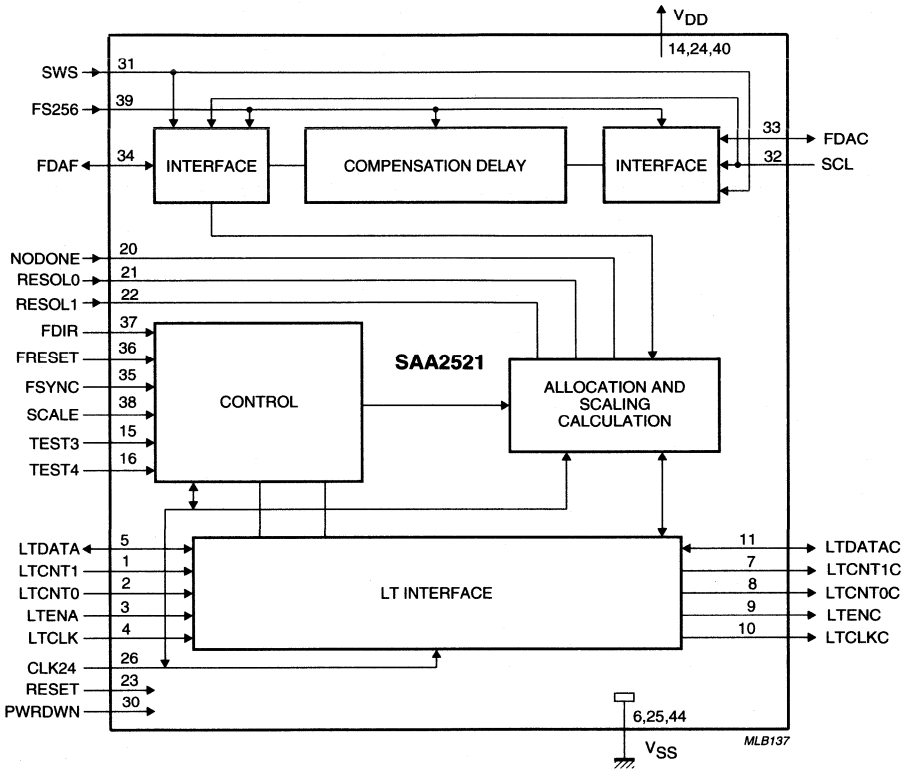


Fig.1 Block diagram.

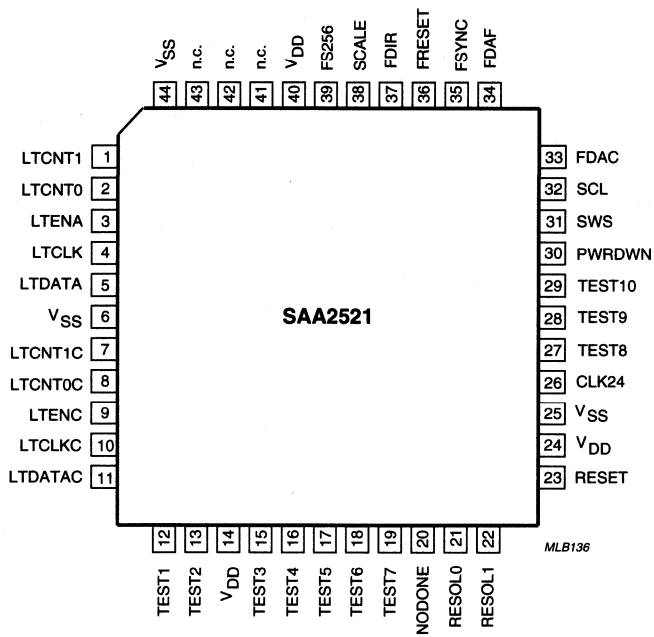


Fig.2 Pin configuration.

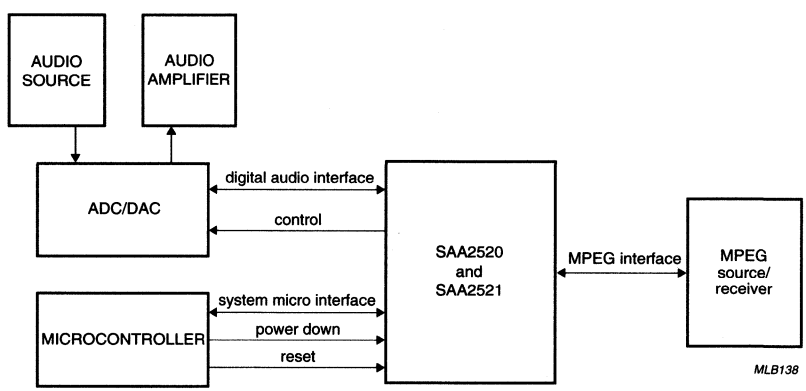


Fig.3 MPEG codec system data flow diagram.

PINNING

SYMBOL	PIN	DESCRIPTION	TYPE
LTCNT1	1	mode control 1, microcontroller interface input	I
LTCNT0	2	mode control 0, microcontroller interface input	I
LTENA	3	enable microcontroller interface input	I
LTCLK	4	bit clock microcontroller interface input	I
LTDATA	5	data, microcontroller interface (3-state inputs/outputs)	I/O
V_{SS}	6	supply ground (0 V)	
LTCNT1C	7	control 1; microcomputer interface	O
LTCNT0C	8	control 0; microcomputer interface	O
LTENC	9	enable microcontroller interface	O
LTCLKC	10	bit clock; microcontroller interface	O
LTDATAC	11	data; microcontroller interface, (3-state inputs/outputs)	I/O
TEST1	12	test output; do not connect	
TEST2	13	test output; do not connect	
V_{DD}	14	positive supply voltage (+ 5 V)	
TEST3	15	test mode input; to be connected to V_{DD}	
TEST4	16	test mode input; to be connected to V_{DD}	
TEST5	17	test input; to be connected to V_{SS}	
TEST6	18	test input; to be connected to V_{SS}	
TEST7	19	test input; to be connected to V_{SS}	
NODONE	20	no done state selection input	I
RESOL0	21	resolution selection 0 input	I
RESOL1	22	resolution selection 1 input	I
RESET	23	active HIGH reset input	I
V_{DD}	24	positive supply voltage (+ 5 V)	
V_{SS}	25	supply ground (0 V)	
CLK24	26	24.576 MHz processing clock input	I
TEST8	27	test input; to be connected to V_{SS}	
TEST9	28	test input; to be connected to V_{SS}	
TEST10	29	test input; to be connected to V_{SS}	
PWRDWN	30	power-down input	I
SWS	31	word selection input; (Filtered) - I^2S-interface	I
SCL	32	bit clock input; (Filtered) - I^2S-interface	I
FDAC	33	filtered data (Filtered) - I^2S-interface (3-state inputs/outputs)	I/O
FDAF	34	filtered data (Filtered) - I^2S-interface (3-state inputs/outputs)	I/O
FSYNC	35	sub-band synchronization on (Filtered) - I^2S-interface, input	I
FRESET	36	reset signal input from SAA2520	I
FDIR	37	direction of the I^2S-interface; input	I
SCALE	38	scale factor index select (note 1)	I
FS256	39	system clock input; sample frequency × 256	I
V_{DD}	40	positive supply voltage (+ 5 V)	

SYMBOL	PIN	DESCRIPTION	TYPE
n.c.	41	not connected	
n.c.	42	not connected	
n.c.	43	not connected	
V_{SS}	44	supply ground (0 V)	

Note to the Pinning Description

1. The scale input must be set LOW for use with the SAA2521.

Digital Video Encoder (ConDENC) SAA7120; SAA7121

FEATURES

- Monolithic CMOS 3.3 V (5 V) device
- Digital PAL/NTSC encoder
- System pixel frequency 13.5 MHz
- Accepts MPEG decoded data on 8-bit wide input port; input data format Cb-Y-Cr (CCIR 656), SAV and EAV
- Three DACs for Y, C and CVBS, two times oversampled with 10 bit resolution
- Real time control of subcarrier
- Cross colour reduction filter
- Closed captioning encoding and WST- and NABTS-Teletext encoding including sequencer and filter
- Line 23 wide screen signalling encoding
- Fast I²C-bus control port (400 kHz)
- Encoder can be master or slave
- Programmable horizontal and vertical input synchronization phase
- Programmable horizontal sync output phase
- Internal colour bar generator (CBG)
- 2 × 2 bytes in lines 20 (NTSC) for copy guard management system can be loaded via I²C-bus
- Down-mode of DACs
- Controlled rise/fall times of synchronization and blanking output signals

- Macrovision Pay-per-View copy protection system rev.7 and rev.6.1 as option.

  This applies to SAA7120 only. The device is protected by USA patent numbers 4631603, 4577216 and 4819098 and other intellectual property rights. Use of the Macrovision anti-copy process in the device is licensed for non-commercial home use only. Reverse engineering or disassembly is prohibited. Please contact your nearest Philips Semiconductors sales office for more information.
- QFP44 package.

GENERAL DESCRIPTION

The SAA7120; SAA7121 encodes digital YUV video data to an NTSC or PAL CVBS or S-Video signal.

The circuit accepts CCIR compatible YUV data with 720 active pixels per line in 4 : 2 : 2 multiplexed formats, for example MPEG decoded data. It includes a sync/clock generator and on-chip DACs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage	3.1	3.3	3.5	V
V_{DDD}	digital supply voltage	3.0	3.3	3.6	V
I_{DDA}	analog supply current	–	–	62	mA
I_{DDD}	digital supply current	–	–	38	mA
V_i	input signal voltage levels	TTL compatible			
$V_{o(p-p)}$	analog output signal voltages Y, C, and CVBS without load (peak-to-peak value)	1.2	1.35	1.45	V
R_L	load resistance	75	–	300	Ω
ILE	LF integral linearity error	–	–	±3	LSB
DLE	LF differential linearity error	–	–	±1	LSB
T_{amb}	operating ambient temperature	0	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7120; SAA7121	QFP44	plastic quad flat package; 44 leads (lead length 2.35 mm); body 10 × 10 × 1.75 mm	SOT307-2

BLOCK DIAGRAM

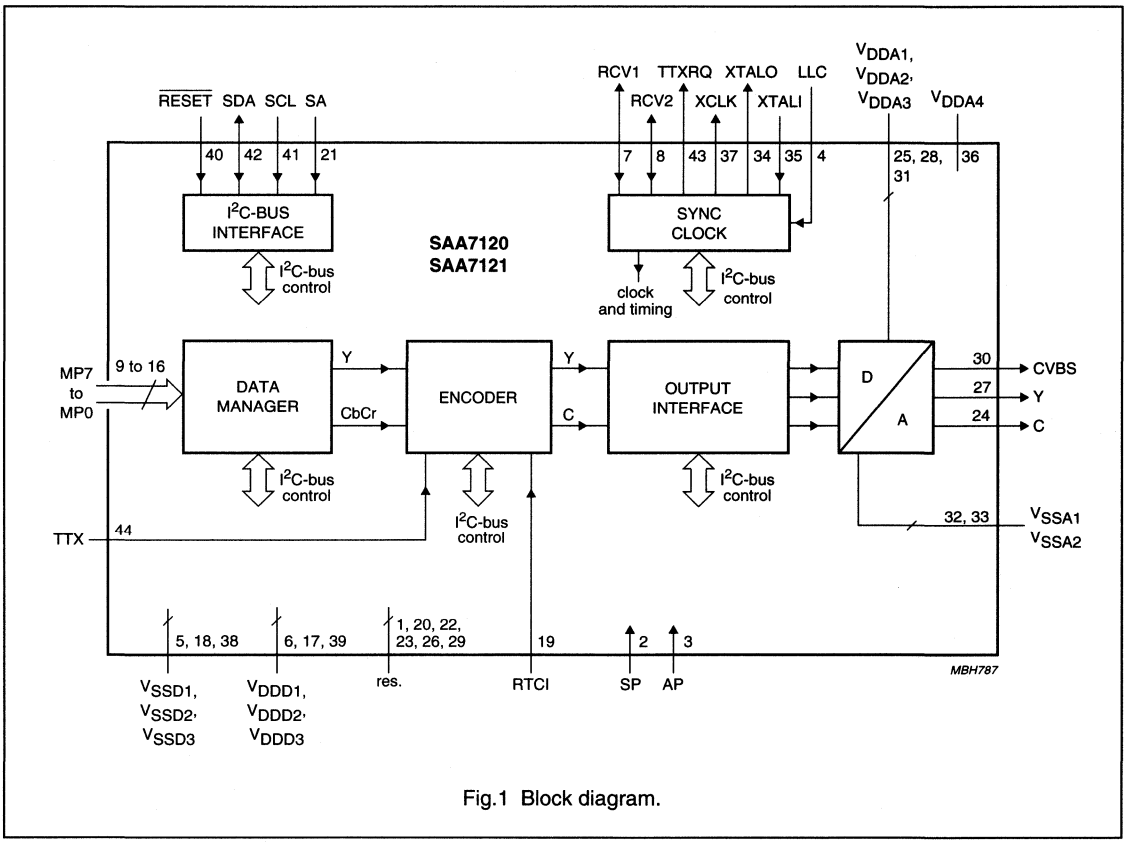


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
res.	1	–	reserved
SP	2	I	test pin; connected to digital ground for normal operation
AP	3	I	test pin; connected to digital ground for normal operation
LLC	4	I	line-locked clock; this is the 27 MHz master clock for the encoder
V_{SSD1}	5	I	digital ground 1
V_{DDD1}	6	I	digital supply voltage 1
RCV1	7	I/O	raster control 1 for video port; this pin receives/provides a VS/FS/FSEQ signal
RCV2	8	I/O	raster control 2 for video port; this pin provides an HS pulse of programmable length or receives an HS pulse
MP7	9	I	MPEG port; it is an input for *"CCIR 656"* style multiplexed Cb Y, Cr data
MP6	10	I	
MP5	11	I	
MP4	12	I	
MP3	13	I	
MP2	14	I	
MP1	15	I	
MP0	16	I	
V_{DDD2}	17	I	digital supply voltage 2
V_{SSD2}	18	I	digital ground 2
RTCI	19	I	Real Time Control input; if the LLC clock is provided by an SAA7111 or SAA7151B, RTCI should be connected to pin RTCO of the decoder to improve the signal quality
res.	20	–	reserved
SA	21	I	the I^2C-bus slave address select input pin; LOW: slave address = 88H, HIGH = 8CH
res.	22	–	reserved
res.	23	–	reserved
C	24	O	analog output of the chrominance signal
V_{DDA1}	25	I	analog supply voltage 1 for the C DAC
res.	26	–	reserved
Y	27	O	analog output of VBS signal
V_{DDA2}	28	I	analog supply voltage 2 for the Y DAC
res.	29	–	reserved
CVBS	30	O	analog output of the CVBS signal
V_{DDA3}	31	I	analog supply voltage 3 for the CVBS DAC
V_{SSA1}	32	I	analog ground 1 for the DACs
V_{SSA2}	33	I	analog ground 2 for the oscillator and reference voltage
XTALO	34	O	crystal oscillator output (to crystal)
XTALI	35	I	crystal oscillator input (from crystal); if the oscillator is not used, this pin should be connected to ground
V_{DDA4}	36	I	analog supply voltage 4 for the oscillator and reference voltage
XCLK	37	O	clock output of the crystal oscillator

SYMBOL	PIN	I/O	DESCRIPTION
V_{SSD3}	38	I	digital ground 3
V_{DDD3}	39	I	digital supply voltage 3
$\overline{RESET}$	40	I	reset input, active LOW; after reset is applied, all digital I/Os are in input mode; the I^2C-bus receiver waits for the START condition
SCL	41	I	I^2C-bus serial clock input
SDA	42	I/O	I^2C-bus serial data input/output
TTXRQ	43	O	teletext request output, indicating when bit stream is valid
TTX	44	I	teletext bit stream input

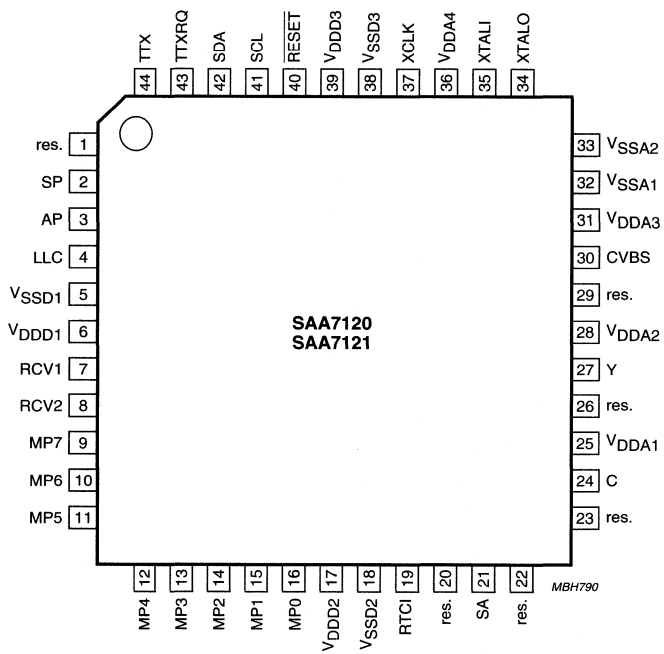


Fig.2 Pin configuration.

DSP for CD and DVD-ROM systems SAA7335

FEATURES

- Compatibility with CD-I, CD-ROM, MPEG-video DVD-ROM and DVD-video applications
- Designed for very high playback speeds
- Typical CD-ROM operation up to n = 12, DVD-ROM to n = 1.9, maximum rates (tbf)
- Matched filtering, quad-pass error correction (C1-C2-C1-C2), overspeed audio playback function included (up to 3 kbytes buffer)
- Lock-to-disc playback, Constant Angular Velocity (CAV), pseudo-Constant Linear Velocity (CLV) and CLV motor control loops
- Interface to 32 kbytes SRAM for DVD error correction and de-interleave
- Sub-code/ header processing for DVD and CD formats
- Programmable HF equalizer
- In DVD mode it is still compatible with Philips block decoders
- Sub-CPU interface can be parallel or fast I²C-bus
- On-chip clock multiplier.

GENERAL DESCRIPTION

This device is a high-end combined Compact Disc (CD) and Digital Versatile Disc (DVD) compatible decoding device. The device operates with an external 32 kbytes S-RAM memory for de-interleaving operations. The device provides quad-pass error correction for CD-ROM applications (C1-C2-C1-C2) and operates in lock-to-disk, CAV, pseudo CLV and CLV modes.

In DVD modes double-pass C1-C2 error correction is used which is capable of correcting up to 5 C1 frame errors and 16 C2 frame errors.

The SAA7335 contains all the functions required to decode an EFM or EFM+ HF signal directly from the laser pre-amplifier, including analog front-end, PLL data recovery, demodulation and error correction. The spindle motor interface provides both motor control signals from the demodulator and, in addition, contains a tachometer loop that accepts tachometer pulses from the motor unit.

The SAA7335 has two independent microcontroller interfaces. The first is a serial I²C-bus and the second is a standard 8-bit multiplexed parallel interface. Both of these interfaces provide access to a total of 32 × 8-bit registers for control and status.

This data sheet contains an descriptive overview of the device together with electrical and timing characteristics. For a detailed description of the device refer to the user guide *"SAU/UM96018"*.

Supply of this CD/DVD IC does not convey an implied license under any patent right to use this IC in any CD or DVD application.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	4.5	5.0	5.5	V
I_{DDD}	digital supply current	–	70	300	mA
V_{DDA}	analog supply voltage	4.5	5.0	5.5	V
I_{DDA}	analog supply current	–	70	300	mA
f_{xtal}	crystal input frequency	4	25	tbf	MHz
T_{amb}	operating ambient temperature	–20	–	+70	°C
T_{stg}	storage temperature	–55	–	+125	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7335GP	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

BLOCK DIAGRAM

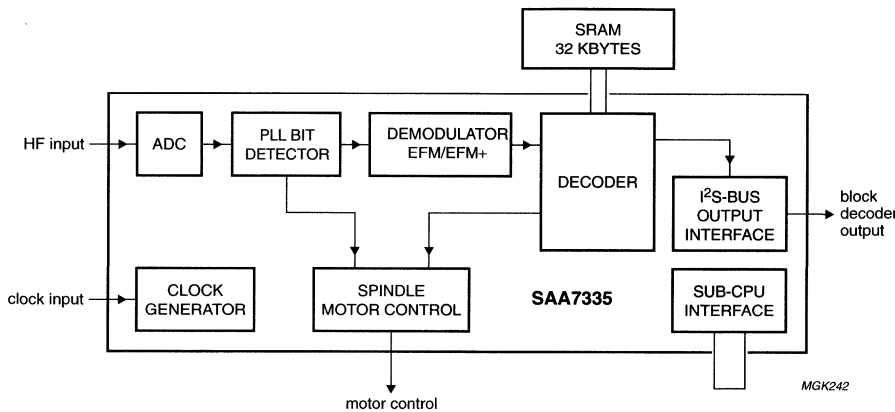


Fig.1 Simplified block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
V_{SSA1}	1	supply	analog ground 1
I_{ref}	2	I	analog current reference input for ADC
REFLo	3	I	analog low reference input for ADC
REFHi	4	I	analog high reference input for ADC
VREF	5	I	analog negative input
HFIN	6	I	analog positive input
V_{SSA2}	7	supply	analog ground 2
AGCOUT	8	O	analog test pin output
V_{DDA2}	9	supply	analog supply voltage 2
V_{DDD1}	10	supply	digital supply voltage 1
V_{SSD1}	11	supply	digital ground 1
OTD	12	I	off track detect input
MOTO1	13	O	3-state motor control output
n.c.	14	–	not connected, reserved
MOTO2/T3	15	I/O	motor control output/tachometer 3 input
n.c.	16	–	not connected, reserved
T1	17	I	tachometer 1 input
T2	18	I	tachometer 2 input
V_{DDD2}	19	supply	digital supply voltage 2
V_{SSD2}	20	supply	digital ground 2
TEST1	21	I	test input 1
TEST2	22	I	test input 2
POR	23	I	power-on reset input
MUXSWICH	24	I	use clock multiplier input
n.c.	25	–	not connected, reserved
CL1	26	O	divided clock output
BCAIN	27	I	BCA input
SDA	28	I/O	sub-CPU I^2C-bus serial data input/output
SCL	29	I	sub-CPU I^2C-bus serial clock input
INT	30	O	sub-CPU interrupt output (open-drain)
V_{DDD3}	31	supply	digital supply voltage 3
V_{SSD3}	32	supply	digital ground 3
da7	33	I/O	sub-CPU data bus bit 7 input/output (parallel)
da6	34	I/O	sub-CPU data bus bit 6 input/output (parallel)
da5	35	I/O	sub-CPU data bus bit 5 input/output (parallel)
n.c.	36	–	not connected, reserved
da4	37	I/O	sub-CPU data bus bit 4 input/output (parallel)
n.c.	38	–	not connected, reserved
da3	39	I/O	sub-CPU data bus bit 3 input/output (parallel)
da2	40	I/O	sub-CPU data bus bit 2 input/output (parallel)

SYMBOL	PIN	TYPE	DESCRIPTION
da1	41	I/O	sub-CPU data bus bit 1 input/output (parallel)
n.c.	42	–	not connected, reserved
da0	43	I/O	sub-CPU data bus bit 0 input/output (parallel)
V_{DDD4}	44	supply	digital supply voltage 4
V_{SSD4}	45	supply	digital ground 4
$\overline{WRi}$	46	I	sub-CPU write enable input (active LOW)
$\overline{RDi}$	47	I	sub-CPU read enable input (active LOW)
ALE	48	I	sub-CPU address latch enable input
CSi	49	I	sub-CPU chip select input (active HIGH)
STOPCLOCK	50	O	stop clock output
n.c.	51	–	not connected, reserved
V4	52	O	serial subcode output (for CD)
EBUOUT	53	O	digital audio output
SYNC	54	O	I^2S-bus sector sync output
FLAG	55	O	I^2S-bus correction flag output
DATA	56	O	I^2S-bus serial data output
BCLK	57	I/O	I^2S-bus bit serial clock input/output
WCLK	58	I/O	I^2S-bus word clock input/output
V_{DDD5}	59	supply	digital supply voltage 5
V_{SSD5}	60	supply	digital ground 5
RAMRW	61	O	RAM read/write control output
n.c.	62	–	not connected, reserved
RAMDA7	63	I/O	RAM data bus bit 7 input/output
RAMDA6	64	I/O	RAM data bus bit 6 input/output
RAMDA5	65	I/O	RAM data bus bit 5 input/output
RAMDA4	66	I/O	RAM data bus bit 4 input/output
RAMDA3	67	I/O	RAM data bus bit 3 input/output
RAMDA2	68	I/O	RAM data bus bit 2 input/output
n.c.	69	–	not connected, reserved
RAMDA1	70	I/O	RAM data bus bit 1 input/output
RAMDA0	71	I/O	RAM data bus bit 0 input/output
V_{DDD6}	72	supply	digital supply voltage 6
V_{SSD6}	73	supply	digital ground 6
RAMAD0	74	O	RAM address bit 0 output
RAMAD1	75	O	RAM address bit 1 output
RAMAD2	76	O	RAM address bit 2 output
RAMAD3	77	O	RAM address bit 3 output
RAMAD4	78	O	RAM address bit 4 output
RAMAD5	79	O	RAM address bit 5 output
RAMAD6	80	O	RAM address bit 6 output
V_{DDD7}	81	supply	digital supply voltage 7

SYMBOL	PIN	TYPE	DESCRIPTION
V_{SSD7}	82	supply	digital ground 7
RAMAD7	83	O	RAM address bit 7 output
RAMAD8	84	O	RAM address bit 8 output
RAMAD9	85	O	RAM address bit 9 output
n.c.	86	–	not connected, reserved
RAMAD10	87	O	RAM address bit 10 output
RAMAD11	88	O	RAM address bit 11 output
RAMAD12	89	O	RAM address bit 12 output
RAMAD13	90	O	RAM address bit 13 output
RAMAD14	91	O	RAM address bit 14 output
V_{DDD8}	92	supply	digital supply voltage 8
V_{SSD8}	93	supply	digital ground 8
CRIN	94	I	analog crystal input
CROUT	95	O	analog crystal output
CFLG	96	O	correction statistics output
MEAS1	97	O	front-end telemetry output
V_{DDD9}	98	supply	digital supply voltage 9
V_{SSD9}	99	supply	digital ground 9
V_{DDA1}	100	supply	analog supply voltage 1

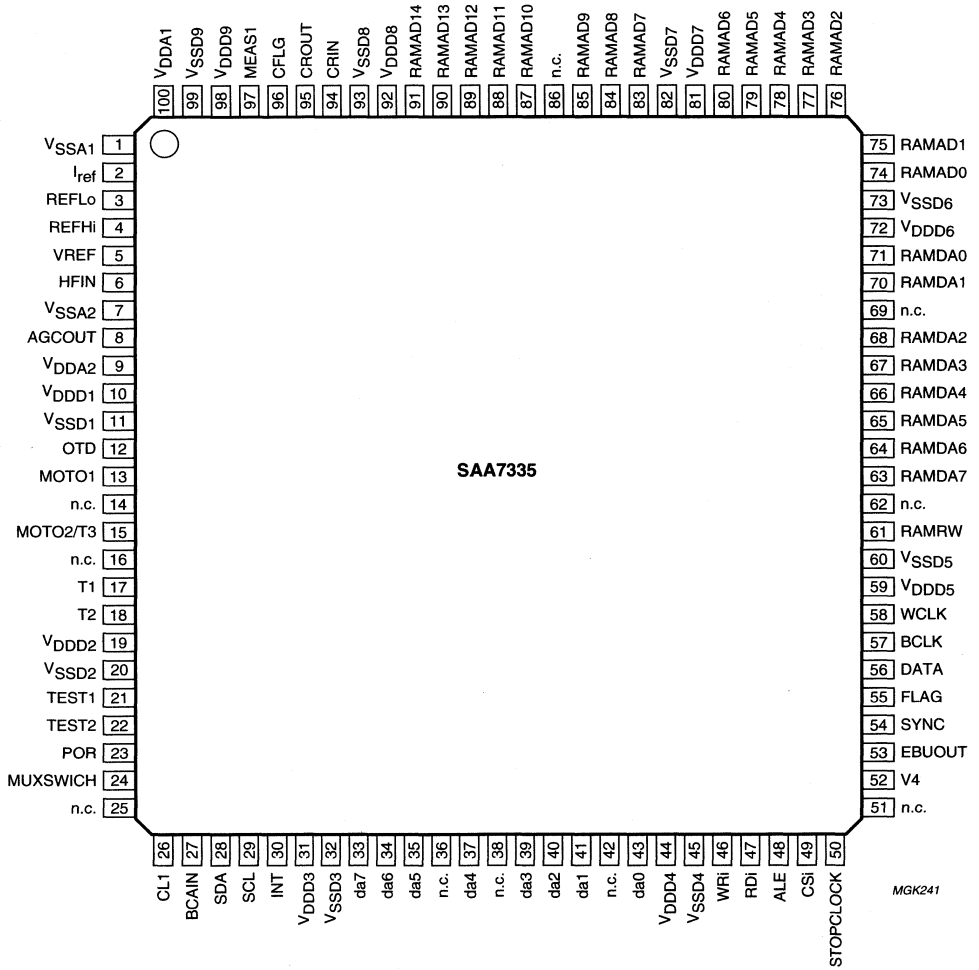


Fig.2 Pin configuration.

CMOS digital decoding IC with RAM for Compact Disc

SAA7345

FEATURES

- Integrated data slicer and clock regenerator
- Digital Phase-Locked Loop (PLL)
- Demodulator and Eight-to-Fourteen Modulation (EFM) decoding
- Subcoding microcontroller serial interface
- Integrated programmable motor speed control
- Error correction and concealment functions
- Embedded Static Random Access Memory (SRAM) for de-interleave and First-In First-Out (FIFO)
- FIFO overflow concealment for rotational shock resistance
- Digital audio interface [European Broadcasting Union (EBU)]
- 2 to 4 times oversampling integrated digital filter
- Audio data peak level detection
- Versatile audio data serial interface
- Digital de-emphasis filter
- Kill interface for Digital-to-Analog Converter (DAC) deactivation during digital silence
- Double speed mode
- Compact Disc Read Only Memory (CD-ROM) modes
- A single speed only version is available (SAA7345GP/SS).

GENERAL DESCRIPTION

The SAA7345 incorporates the CD signal processing functions of decoding and digital filtering. The device is equipped with on-board SRAM and includes additional features to reduce the processing required in the analog domain.

Supply of this Compact Disc IC does not convey an implied license under any patent right to use this IC in any Compact Disc application.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	3.4	5.0	5.5	V
I_{DD}	supply current	–	22	50	mA
f_{xtal}	crystal frequency	8	16.9344 or 33.8688	35	MHz
T_{amb}	operating ambient temperature	−40	–	+85	°C
T_{stg}	storage temperature	−55	–	+125	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7345GP	QFP44	plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 × 14 × 2.2 mm	SOT205-1

BLOCK DIAGRAM

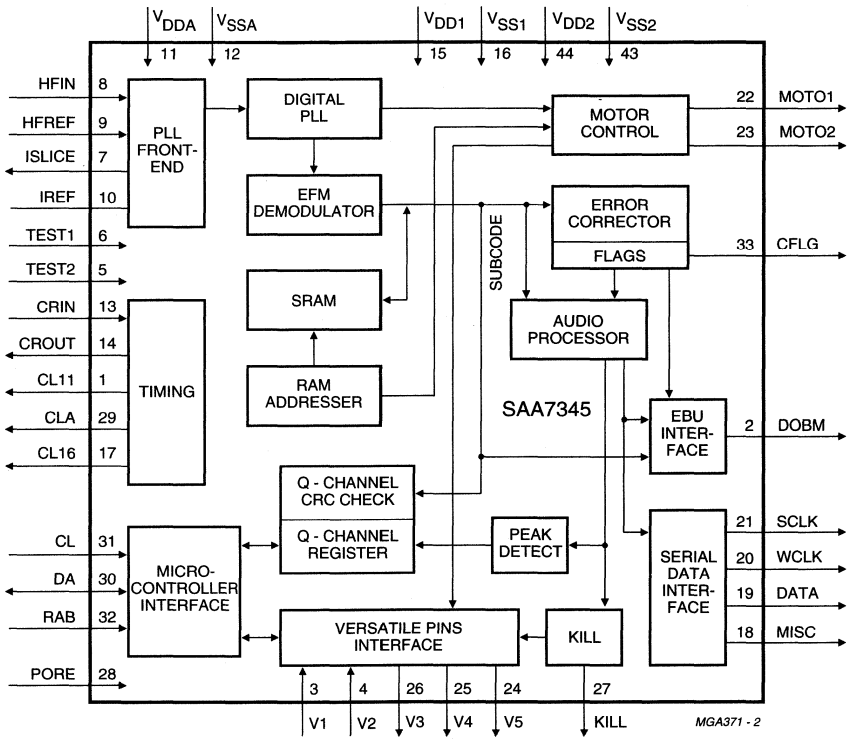


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CL11	1	11.2896 or 5.6448 MHz clock output (3-state); (divide-by-3)
DOBM	2	bi-phase mark output (externally buffered; 3-state)
V1	3	versatile input pin
V2	4	versatile input pin
TEST2	5	test input; this pin should be tied LOW
TEST1	6	test input; this pin should be tied LOW
ISLICE	7	current feedback output from data slicer
HFIN	8	comparator signal input
HFREF	9	comparator common-mode input
IREF	10	reference current pin (nominally $\frac{1}{2}V_{DD}$)
V_{DDA}	11	analog supply voltage; note 1
V_{SSA}	12	analog ground; note 1
CRIN	13	crystal/resonator input
CROUT	14	crystal/resonator output
V_{DD1}	15	digital supply to input and output buffers; note 1
V_{SS1}	16	digital ground to input and output buffers; note 1
CL16	17	16.9344 MHz system clock output
MISC	18	general purpose DAC output (3-state)
DATA	19	serial data output (3-state)
WCLK	20	word clock output (3-state)
SCLK	21	serial bit clock output (3-state)
MOTO1	22	motor output 1; versatile (3-state)
MOTO2	23	motor output 2; versatile (3-state)
V5	24	versatile output pin
V4	25	versatile output pin
V3	26	versatile output pin (open-drain)
KILL	27	kill output; programmable (open-drain)
$\overline{PORE}$	28	power-on reset enable input (active LOW)
CLA	29	4.2336 MHz microcontroller clock output
DA	30	interface data I/O line
CL	31	interface clock input line
RAB	32	interface R/$\overline{W}$ and acknowledge input
CFLG	33	correction flag output (open-drain)
n.c.	34 to 42	no internal connection
V_{SS2}	43	digital ground to internal logic; note 1
V_{DD2}	44	digital supply voltage to internal logic; note 1

Note

1. All supply pins must be connected to the same external power supply.

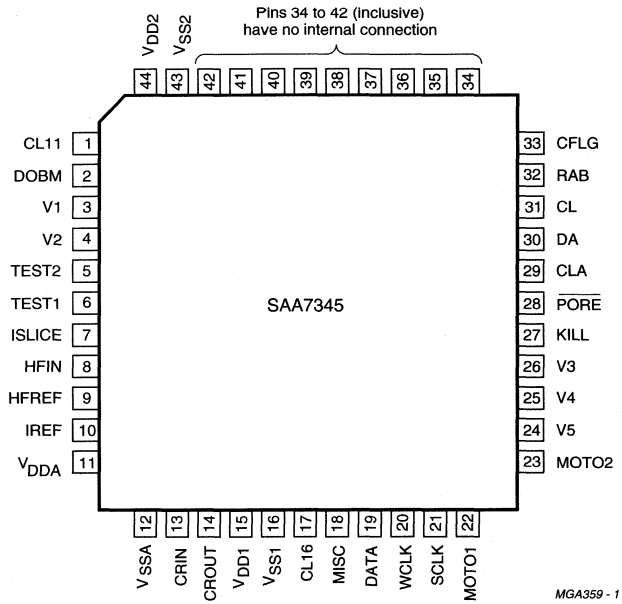


Fig.2 Pin configuration.

CONTENTS

1 FEATURES

- Focus servo loop
- Radial servo loop
- Built-in access procedure with fast track count possibilities
- Sledge motor servo loop with pulsed sledge support
- High speed error correction, up to sixteen times over-speed
- Supports three different over-speed ranges with only one external crystal
- Lock-to-disc mode
- Full turntable motor control
- Full error correction strategy, t = 2 and e = 4
- All standard decoder functions implemented digitally
- Adaptive digital HF equalizer
- FIFO overflow concealment for rotational shock resistance
- Digital audio interface (EBU), audio and data
- 2 and 4 times oversampling integrated digital filter, including f_s mode
- Audio data peak level detection
- Kill interface for DAC deactivation during digital silence
- All TDA1301 (DSIC2) digital servo functions
- Low focus noise
- Improved playability on ABEX TCD-721R, TCD-725 and TCD-714 discs
- Automatic closed loop gain control available for focus and radial loops
- On chip clock multiplier allows the use of 8.4672 MHz crystal
- S2B serial interface with host controller
- Double speed servo
- Integrated engine controller (high speed embedded 80C51)
- External program support.

2 GENERAL DESCRIPTION

The SAA7348 All Compact Disc Engine (ACE) combines the functionality of a CD decoder (LO9585), a digital servo (OQ8868) and a microcontroller core (80C51 based) on a single chip. It was developed for high speed CD-ROM applications but, due to the large scale integration, can also be used in other CD applications. The internal microcontroller makes it possible to develop other applications quickly. The microcontroller can operate with internal or external ROM.

Additional features include:

- High level integration
- Improved communication speed.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7348GP	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

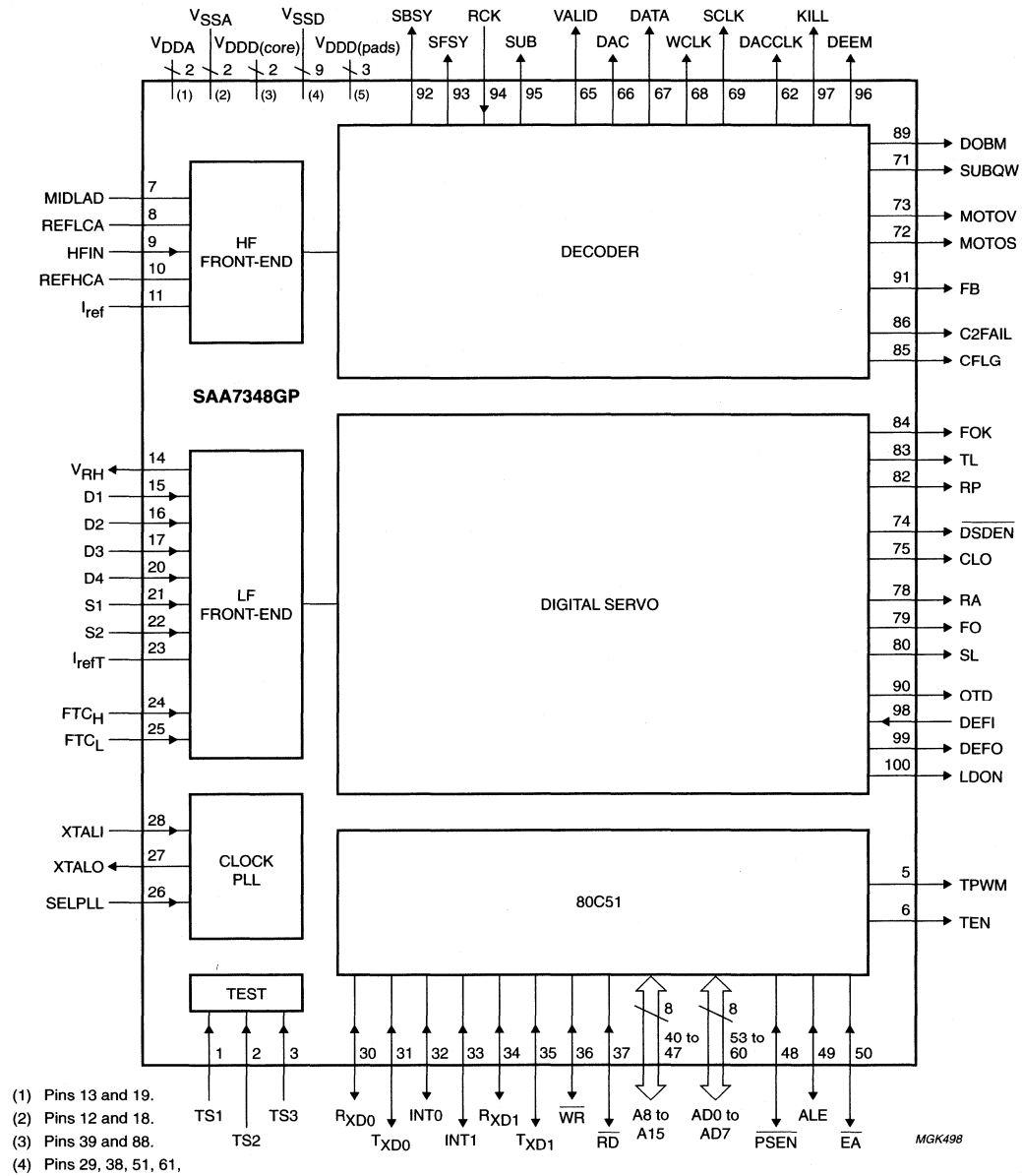
4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DDD(pads)}$	digital supply voltage for pad cells		4.5	5.0	5.5	V
$V_{DDD(core)}$	digital supply voltage for the core	note 1	3.0	3.3	3.6	V
V_{DDA}	analog supply voltage	note 1	3.0	3.3	3.6	V
I_{DD}	supply current	n = 8 mode	–	90	–	mA
f_{xtal}	crystal frequency		8	8.4672	35	MHz
T_{amb}	operating ambient temperature		0	–	70	°C
T_{stg}	storage temperature		−55	–	+125	°C

Note

1. The analog and digital core supply pins (V_{DDA} and $V_{DDD(core)}$) must be connected to the same external supply. The core and pads can operate at different voltages and should never be connected together directly.

5 BLOCK DIAGRAM



(1) Pins 13 and 19.
(2) Pins 12 and 18.
(3) Pins 39 and 88.
(4) Pins 29, 38, 51, 61, 63, 70, 76, 81 and 87.
(5) Pins 52, 64 and 77.

Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	TYPE[1]	DESCRIPTION
TS1	1	I	test control input; this pin should be tied LOW
TS2	2	I	test control input; this pin should be tied LOW
TS3	3	I	test control input; this pin should be tied LOW
RST	4	I	power-on reset input
TPWM	5	O	tray PWM output
TEN	6	O	tray enable output
MIDLAD	7	A	ladder middle decoupling of High Frequency (HF) ADC
REFLCA	8	A	ladder low decoupling of HF ADC
HFIN	9	A	HF input
REFHCA	10	A	ladder high decoupling of HF ADC
I_{ref}	11	A	reference current input
V_{SSA1}	12	S	analog ground 1 for HF front-end
V_{DDA1}	13	S	analog supply voltage 1 for HF front-end (3.3 V)
V_{RH}	14	A	calibrated reference voltage output from ADC
D1	15	A	unipolar current input (central diode signal input)
D2	16	A	unipolar current input (central diode signal input)
D3	17	A	unipolar current input (central diode signal input)
V_{SSA2}	18	S	analog ground 2 for LF front-end
V_{DDA2}	19	S	analog supply voltage 2 for LF front-end (3.3 V)
D4	20	A	unipolar current input (central diode signal input)
S1	21	A	unipolar current input (satellite diode signal input)
S2	22	A	unipolar current input (satellite diode signal input)
I_{refT}	23	A	current reference, for input range of LF front-end ADCs
FTC_H	24	A	fast track counter comparator (+) input
FTC_L	25	A	fast track counter comparator (–) input
SELPLL	26	I	enables internal clock multiplier PLL
XTALO	27	A	crystal output
XTALI	28	A	crystal input
V_{SSD1}	29	S	digital ground 1
R_{XD0}	30	B	P3.0
T_{XD0}	31	B	P3.1
INT0	32	B	P3.2 (interrupt 0)
INT1	33	B	P3.3 (interrupt 1)
R_{XD1}	34	B	P3.4
T_{XD1}	35	B	P3.5
$\overline{WR}$	36	B	P3.6; active LOW
$\overline{RD}$	37	B	P3.7; active LOW
V_{SSD2}	38	S	digital ground 2
$V_{DDD1(core)}$	39	S	digital supply voltage 1 for the core (3.3 V)
A8	40	B	P2.0 (address or I/O)

SYMBOL	PIN	TYPE[1]	DESCRIPTION
A9	41	B	P2.1 (address or I/O)
A10	42	B	P2.2 (address or I/O)
A11	43	B	P2.3 (address or I/O)
A12	44	B	P2.4 (address or I/O)
A13	45	B	P2.5 (address or I/O)
A14	46	B	P2.6 (address or I/O)
A15	47	B	P2.7 (address or I/O)
$\overline{PSEN}$	48	B	program store enable (pull-up; active LOW)
ALE	49	B	address latch enable (pull-up)
$\overline{EA}$	50	B	external ROM select (active LOW); enhanced hooks
V_{SSD3}	51	S	digital ground 3
$V_{DDD1(pads)}$	52	S	digital supply voltage 1 for the pads (5 V); pins 26 to 60
AD0	53	B	P0.0 (data, address or I/O)
AD1	54	B	P0.1 (data, address or I/O)
AD2	55	B	P0.2 (data, address or I/O)
AD3	56	B	P0.3 (data, address or I/O)
AD4	57	B	P0.4 (data, address or I/O)
AD5	58	B	P0.5 (data, address or I/O)
AD6	59	B	P0.6 (data, address or I/O)
AD7	60	B	P0.7 (data, address or I/O)
V_{SSD4}	61	S	digital ground 4
DACCLK	62	T	BCC-DAC clock output
V_{SSD5}	63	S	digital ground 5
$V_{DDD2(pads)}$	64	S	digital supply voltage 2 (level shifter) for the pads (5 V)
VALID	65	T	data validity flag; C2 error flag; (3-state)
DAC	66	T	serial audio data output to DAC (3-state)
DATA	67	T	serial data output to block decoder (3-state)
WCLK	68	T	word clock output (3-state)
SCLK	69	T	serial bit clock output (3-state)
V_{SSD6}	70	S	digital ground 6
SUBQW	71	O	subcode output; Q to W subcode bits
MOTOS	72	T	motor output, sign
MOTOV	73	T	motor output, value
$\overline{DSDEN}$	74	O	DSD enable output (active LOW)
CLO	75	O	clock output
V_{SSD7}	76	S	digital ground 7
$V_{DDD3(pads)}$	77	S	digital supply voltage 3 for the pads (5 V); pins 1 to 6 and 65 to 100
RA	78	T	radial actuator output
FO	79	T	focus actuator output
SL	80	T	sledge control output
V_{SSD8}	81	S	digital ground 8

SYMBOL	PIN	TYPE[1]	DESCRIPTION
RP	82	OD	radial polarity signal (open drain)
TL	83	OD	track loss signal (open drain)
FOK	84	OD	focus OK signal or decoder measurement signal (open drain)
CFLG	85	OD	correction flag output (open drain)
C2FAIL	86	OD	indication of correction failure (open drain)
V_{SSD9}	87	S	digital ground 9
$V_{DDD2(core)}$	88	S	digital supply voltage 2 for the core (3.3 V)
DOBM	89	T	EBU bi-phase mark output (externally buffered) (3-state)
OTD	90	O	off-track detect
FB	91	OD	FIFO boundary, motor overflow (open drain)
SBSY	92	T	subcode block sync (3-state)
SFSY	93	T	subcode frame sync (3-state)
RCK	94	I	subcode clock input
SUB	95	T	P to W subcode bits (3-state)
DEEM	96	O	deemphasis active output
KILL	97	OD	kill output (open drain)
DEFI	98	I	defect detector input
DEFO	99	O	defect detector output
LDON	100	OD	laser drive on output (open drain)

Note

1. Pin type abbreviations: O = Output, I = Input, S = power Supply, A = Analog function, OD = Open Drain, B = Bidirectional, T = 3-state output. All supply pins must be connected directly to their respective external power supply voltages.

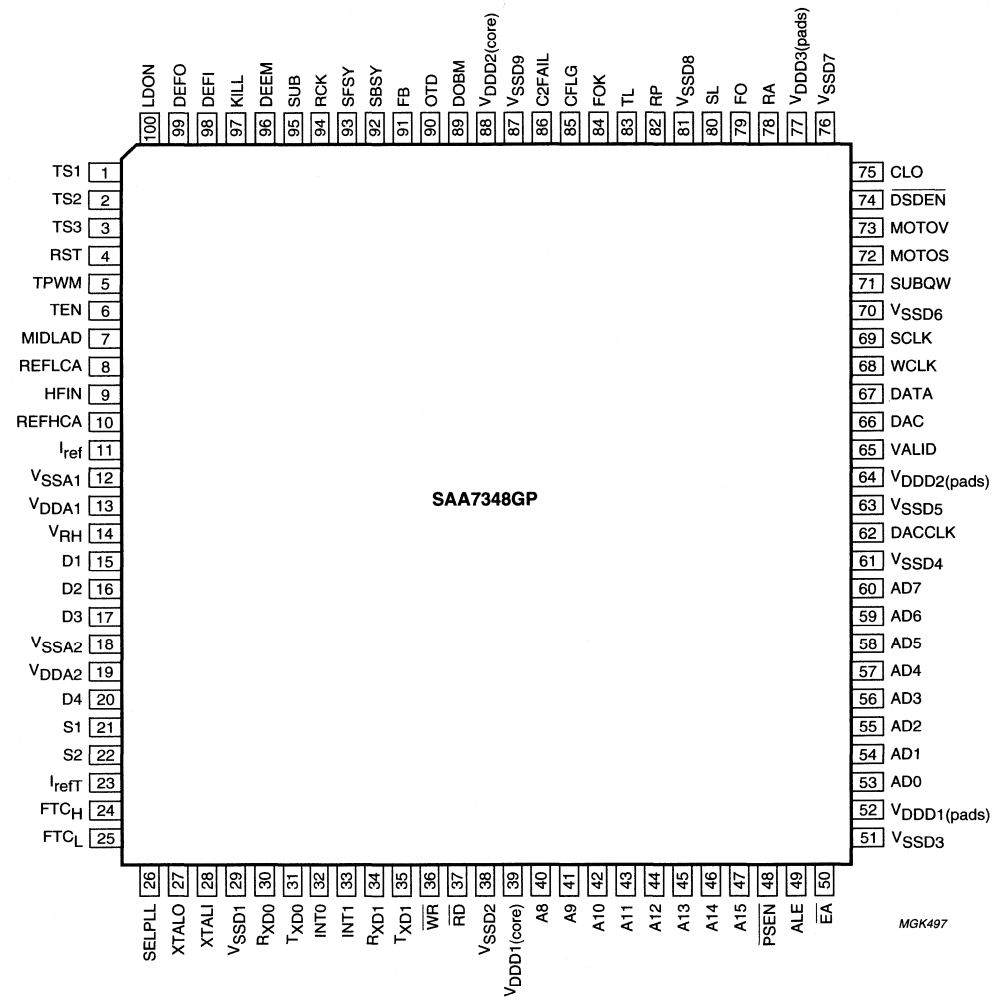


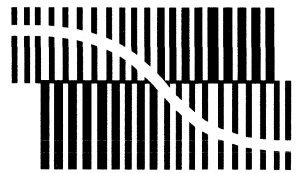
Fig.2 Pin configuration.

Bitstream conversion ADC for digital audio systems

SAA7367

FEATURES

- Total Harmonic Distortion plus Noise (THD + N) = −88 dB (0.004%); DR = 93 dB; S/N = 97 dB
- Simple interfacing to analog inputs
- Small, non-critical PCB layout
- Low pin-out SO24 package (pin-compatible to SAA7366)
- 4 flexible serial interface modes
- 4.5 to 5.5 V operation
- Standby mode
- Detection of digital signal ≥−1 dB amplitude
- Up to 18 significant bits serial output
- Selectable high-pass filter.



BITSTREAM CONVERSION

GENERAL DESCRIPTION

The SAA7367 is a CMOS low-cost stereo Analog-to-Digital Converter (ADC) using the Philips bitstream conversion technique.

APPLICATIONS

The device is designed for the digital acquisition of analog audio signals for digital audio systems such as:

- Compact Disc-Recordable (CD-R)
- Digital Compact Cassette (DCC)
- Digital Audio Tape (DAT).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDD}	digital supply current		–	17	–	mA
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current		–	13	–	mA
f_{BCK}	clock input frequency		4.60	12.288	12.8	MHz
f_s	sample rate		18	48	50	kHz
THD + N	total harmonic distortion plus noise	at 0 dB input	–	−88	−80	dB
DR	dynamic range	at −60 dB	90	93	–	dB
S/N	signal-to-noise ratio		–	97	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7367	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

BLOCK DIAGRAM

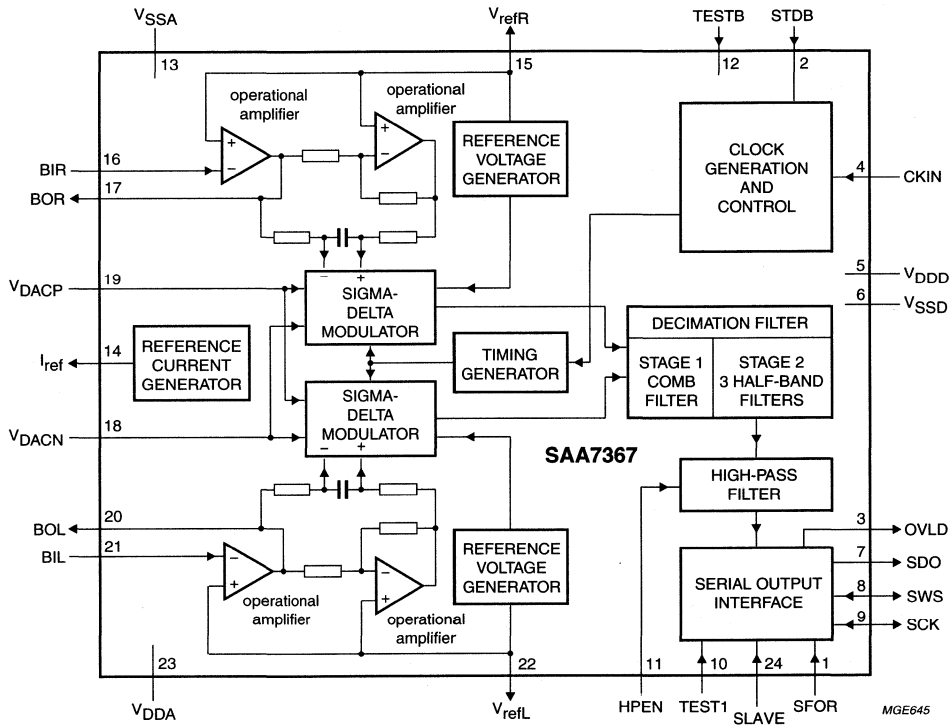


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SFOR	1	TTL level input; in normal mode this input selects the serial interface output format; output format is selected as follows: SFOR = HIGH selects Format 1 SFOR = LOW selects Format 2 (similar to I^2S)
STDB	2	schmitt-trigger input; in normal mode, this input is used to select standby mode:
		STDB = HIGH selects normal operation
		STDB = LOW selects standby mode (low power consumption)
OVLD	3	TTL level output; in normal mode this output indicates whether the internal digital signal is within 1 dB of maximum; if so, the output will go HIGH for 131072 clock cycles (approximately 11 ms); in standby mode this output is forced LOW
CKIN	4	CMOS level input; system clock input; nominally clocked at $256f_s$
V_{DDD}	5	digital supply voltage (4.5 to 5.5 V)
V_{SSD}	6	digital ground
SDO	7	TTL level output (3-state); in normal mode this pin outputs data from the serial interface; in standby mode, this output is high impedance
SWS	8	TTL level input/output; serial interface word select signal; in master mode (SLAVE = LOW), this pin outputs the serial interface word select signal; in slave mode (SLAVE = HIGH), this pin is the word select input to the serial interface; in standby mode (STDB = LOW) this pin is always an input (high impedance); for polarity: see Table 1
SCK	9	TTL level input/output; in master mode (SLAVE = LOW) the pin outputs the serial interface bit clock; in slave mode (SLAVE = HIGH) this pin is the input for the external bit clock; data on SDO is clocked out on the HIGH-to-LOW transition of SCK; the data is valid on the LOW-to-HIGH transition
TEST1	10	Test 1; TTL level input with internal pull-down; in slave mode (slave = HIGH), this pin is used to select extra serial interface formats (see Table 2)
HPEN	11	TTL level input; this input is used to enable the internal high-pass filter when HIGH; in scan-test mode (TESTB = LOW and TEST1 = LOW) this pin functions as 'scan chain c' input
TESTB	12	Test B; CMOS level input with internal pull-up; in normal applications, this input should be left HIGH
V_{SSA}	13	analog ground; this pin is internally connected to V_{SS} via the on-chip substrate contacts
I_{ref}	14	current reference generator output; 33 kΩ in parallel with 22 nF is connected from this pin to V_{SSA}
V_{refR}	15	right channel analog reference output voltage ($\frac{1}{2}V_{DDA}$)
BIR	16	buffer operational amplifier inverting input for right channel
BOR	17	buffer operational amplifier output for right channel
V_{DACN}	18	negative 1-bit DAC reference voltage input, connected to 0 V
V_{DACP}	19	positive 1-bit DAC reference voltage input, connected to +5 V
BOL	20	buffer operational amplifier output for left channel
BIL	21	buffer operational amplifier inverting input for left channel
V_{refL}	22	left channel analog reference output voltage ($\frac{1}{2}V_{DDA}$)
V_{DDA}	23	analog supply voltage (4.5 to 5.5 V)

SYMBOL	PIN	DESCRIPTION
SLAVE	24	TTL level input; used to select the serial interface operating mode: SLAVE = HIGH selects slave mode SLAVE = LOW selects master mode

Table 1 SWS polarity

CONDITIONS			POLARITY
SLAVE AND TEST1	SWS	SFOR	
SLAVE = LOW or TEST1 = LOW	LOW	LOW	left data
	LOW	HIGH	right data
SLAVE = HIGH and TEST1 = HIGH	LOW	LOW	right data
	LOW	HIGH	left data

Table 2 Selection of serial interface formats via TEST1

CONDITIONS		SELECTED FORMAT
SFOR	TEST1	
HIGH	LOW	format 1
	HIGH	format 2
LOW	LOW	format 3
	HIGH	format 4

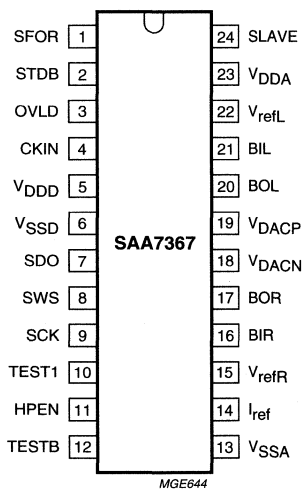
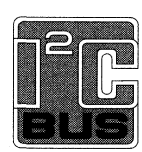


Fig.2 Pin configuration.

Single-chip digital servo processor and Compact Disc decoder (CD7)

SAA7372

CONTENTS



Single-chip digital servo processor and Compact Disc decoder (CD7) SAA7372

1 FEATURES

- CD ROM mode
- Single and double-speed modes
- Lock-to-disc mode
- Full error correction strategy, t = 2 and e = 4
- Full CD graphics interface
- All standard decoder functions implemented digitally on chip
- FIFO overflow concealment for rotational shock resistance
- Digital audio interface (EBU), audio and data
- 2 and 4 times oversampling integrated digital filter, including f_s mode
- Audio data peak level detection
- Kill interface for DAC deactivation during digital silence
- All TDA1301 (DSIC2) digital servo functions, plus extra high-level functions
- Low focus noise
- Improved playability on ABEX TCD-721R, TCD-725 and TCD-714 discs
- Automatic closed loop gain control available for focus and radial loops
- Pulsed sledge support
- Microcontroller loading LOW
- High-level servo control option
- High-level mechanism monitor
- Communication may be via TDA1301/SAA7345 compatible bus or I^2C-bus
- On-chip clock multiplier allows the use of 8.4672 MHz crystal.

2 GENERAL DESCRIPTION

The SAA7372 is a single chip combining the functions of a CD decoder IC and digital servo IC. The decoder part is based on the SAA7345 (CD6) with an improved error correction strategy. The servo part is based on the TDA1301T (DSIC2) with improvements incorporated, extra features have also been added.

Supply of this Compact Disc IC does not convey an implied license under any patent right to use this IC in any Compact Disc application.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.4	5.0	5.5	V
I_{DD}	supply current	n = 1 mode	–	49	–	mA
f_{xtal}	crystal frequency		8	8.4672	35	MHz
T_{amb}	operating ambient temperature		−10	–	+70	°C
T_{stg}	storage temperature		−55	–	+125	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7372	QFP64	plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 × 14 × 2.7 mm	SOT393-1

5 BLOCK DIAGRAM

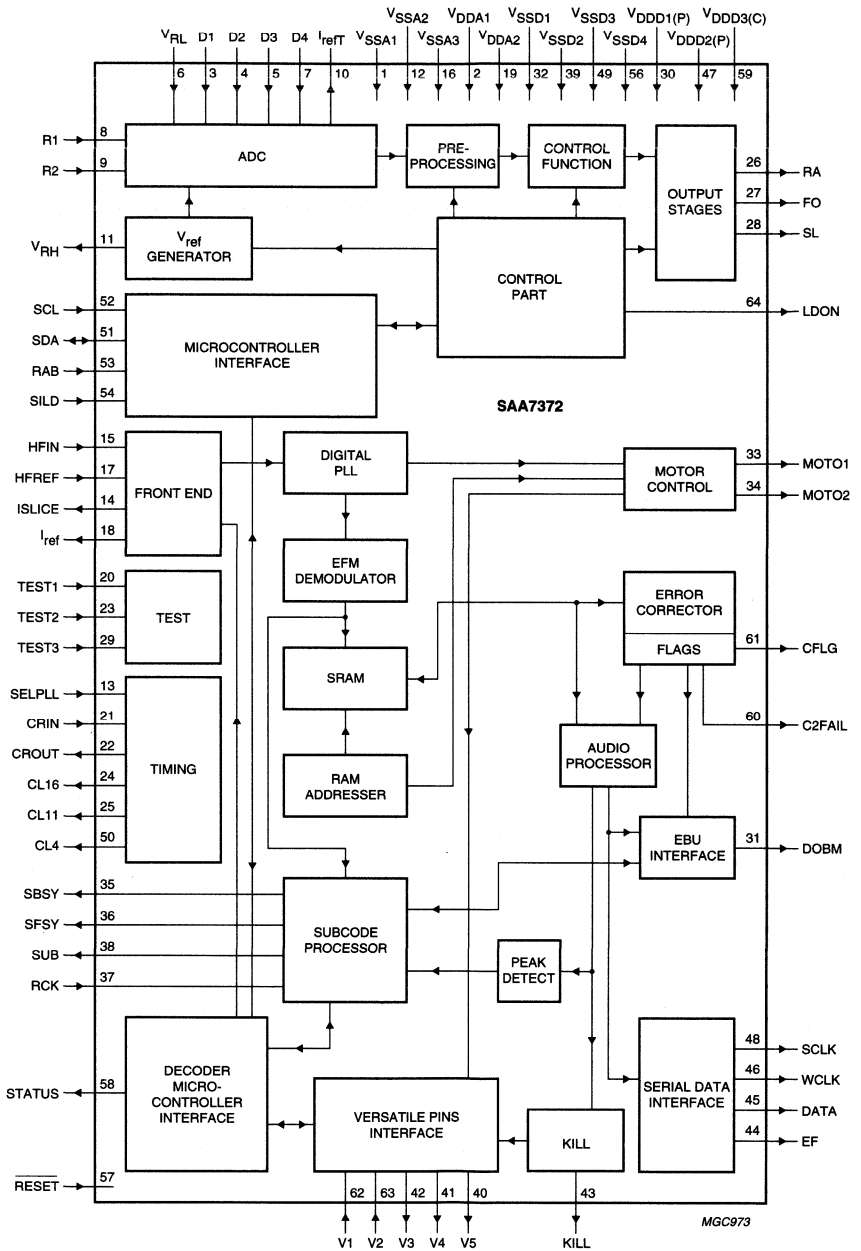


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSA1}	1[1]	analog ground 1
V_{DDA1}	2[1]	analog supply voltage 1
D1	3	unipolar current input (central diode signal input)
D2	4	unipolar current input (central diode signal input)
D3	5	unipolar current input (central diode signal input)
V_{RL}	6	reference voltage input for ADC
D4	7	unipolar current input (central diode signal input)
R1	8	unipolar current input (satellite diode signal input)
R2	9	unipolar current input (satellite diode signal input)
I_{refT}	10	current reference output for ADC calibration
V_{RH}	11	reference voltage output from ADC
V_{SSA2}	12[1]	analog ground 2
SELPLL	13	selects whether internal clock multiplier PLL is used
ISLICE	14	current feedback output from data slicer
HFIN	15	comparator signal input
V_{SSA3}	16[1]	analog ground 3
HFREF	17	comparator common mode input
I_{ref}	18	reference current output pin (nominally $0.5V_{DD}$)
V_{DDA2}	19[1]	analog supply voltage 2
TEST1	20	test control input 1; this pin should be tied LOW
CRIN	21	crystal/resonator input
CROUT	22	crystal/resonator output
TEST2	23	test control input 2; this pin should be tied LOW
CL16	24	16.9344 MHz system clock output
CL11	25	11.2896 or 5.6448 MHz clock output (3-state)
RA	26	radial actuator output
FO	27	focus actuator output
SL	28	sledge control output
TEST3	29	test control input 3; this pin should be tied LOW
$V_{DDD1(P)}$	30[1]	digital supply voltage 1 for periphery
DOBM	31	bi-phase mark output (externally buffered; 3-state)
V_{SSD1}	32[1]	digital ground 1
MOTO1	33	motor output 1; versatile (3-state)
MOTO2	34	motor output 2; versatile (3-state)
SBSY	35	subcode block sync output (3-state)
SFSY	36	subcode frame sync output (3-state)
RCK	37	subcode clock input
SUB	38	P-to-W subcode output bits (3-state)
V_{SSD2}	39[1]	digital ground 2
V5	40	versatile output pin 5

SYMBOL	PIN	DESCRIPTION
V4	41	versatile output pin 4
V3	42	versatile output pin 3 (open-drain)
KILL	43	kill output (programmable; open-drain)
EF	44	C2 error flag; output only defined in CD ROM modes and $1f_s$ modes (3-state)
DATA	45	serial data output (3-state)
WCLK	46	word clock output (3-state)
$V_{DDD2(P)}$	47[1]	digital supply voltage 2 for periphery
SCLK	48	serial bit clock output (3-state)
V_{SSD3}	49[1]	digital ground 3
CL4	50	4.2336 MHz microcontroller clock output
SDA	51	microcontroller interface data I/O line (open-drain output)
SCL	52	microcontroller interface clock line input
RAB	53	microcontroller interface R/$\overline{W}$ and load control line input (4-wire bus mode)
SILD	54	microcontroller interface $\overline{R}$/W and load control line input (4-wire-bus mode)
n.c.	55	not connected
V_{SSD4}	56[1]	digital ground 4
$\overline{RESET}$	57	power-on reset input (active LOW)
STATUS	58	servo interrupt request line/decoder status register output (open-drain)
$V_{DDD3(C)}$	59[1]	digital supply voltage 3 for core
C2FAIL	60	indication of correction failure output (open-drain)
CFLG	61	correction flag output (open-drain)
V1	62	versatile input pin 1
V2	63	versatile input pin 2
LDON	64	laser drive on output (open-drain)

Note

1. All supply pins must be connected to the same external power supply voltage.

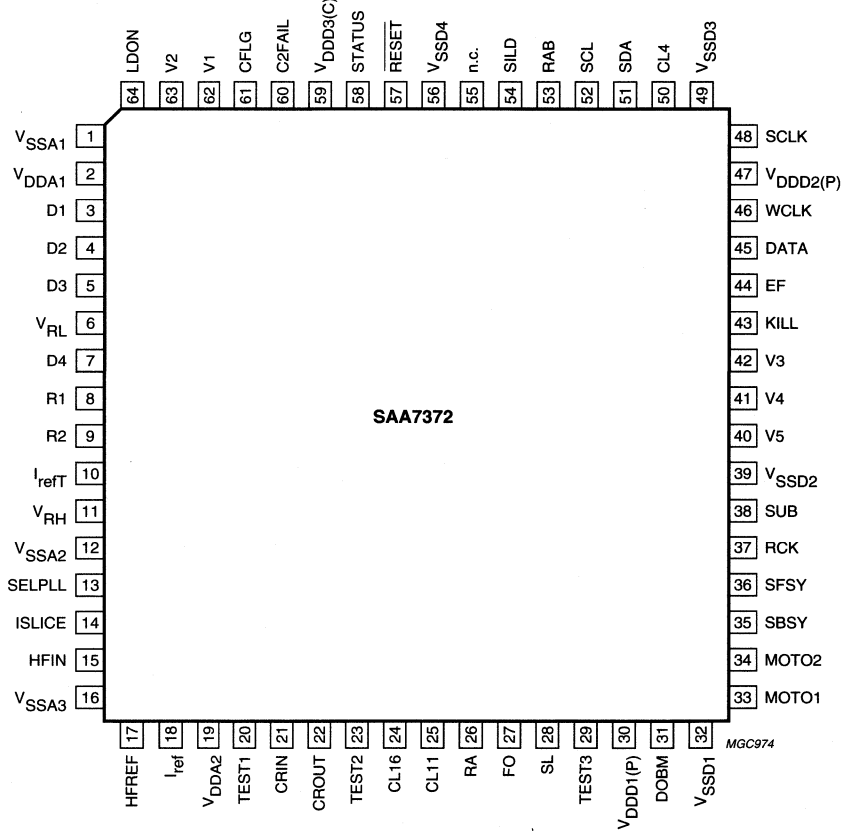
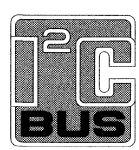


Fig.2 Pin configuration.

Low voltage digital servo processor and Compact Disc decoder (CD7LV) SAA7374

CONTENTS



Low voltage digital servo processor and Compact Disc decoder (CD7LV)

SAA7374

1 FEATURES

- CD-ROM mode
- Single and double-speed modes
- Lock-to-disc mode
- Full error correction strategy, t = 2 and e = 4
- Full CD graphics interface
- All standard decoder functions implemented digitally on chip
- FIFO overflow concealment for rotational shock resistance
- Digital audio interface (EBU), audio and data
- 2 and 4 times oversampling integrated digital filter, including f_s mode
- Audio data peak level detection
- Kill interface for DAC deactivation during digital silence
- All TDA1301 (DSIC2) digital servo functions, plus extra high-level functions
- Low focus noise
- Improved playability on ABEX TCD-721R, TCD-725 and TCD-714 discs
- Automatic closed loop gain control available for focus and radial loops
- Pulsed sledge support
- Microcontroller loading LOW
- High-level servo control option
- High-level mechanism monitor
- Communication may be via TDA1301/SAA7345 compatible bus or I^2C-bus
- On-chip clock multiplier allows the use of 8.4672 MHz crystal.

2 GENERAL DESCRIPTION

The SAA7374 (CD7LV) is a low-voltage chip which combines the functions of a CD decoder IC and Digital Servo IC. The decoder part is based on the SAA7345 (CD6) with an improved error correction strategy. The servo part is based on the TDA1301T (DSIC2) with improvements incorporated. Extra features have also been added.

Supply of this Compact Disc IC does not convey an implied license under any patent right to use this IC in any Compact Disc application.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	3.3	3.6	V
I_{DD}	supply current	n = 1 mode	–	28	–	mA
f_{xtal}	crystal frequency		8	8.4672	35	MHz
T_{amb}	operating ambient temperature		−10	–	+70	°C
T_{stg}	storage temperature		−55	–	+125	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7374	QFP64	plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 × 14 × 2.7 mm	SOT393-1

5 BLOCK DIAGRAM

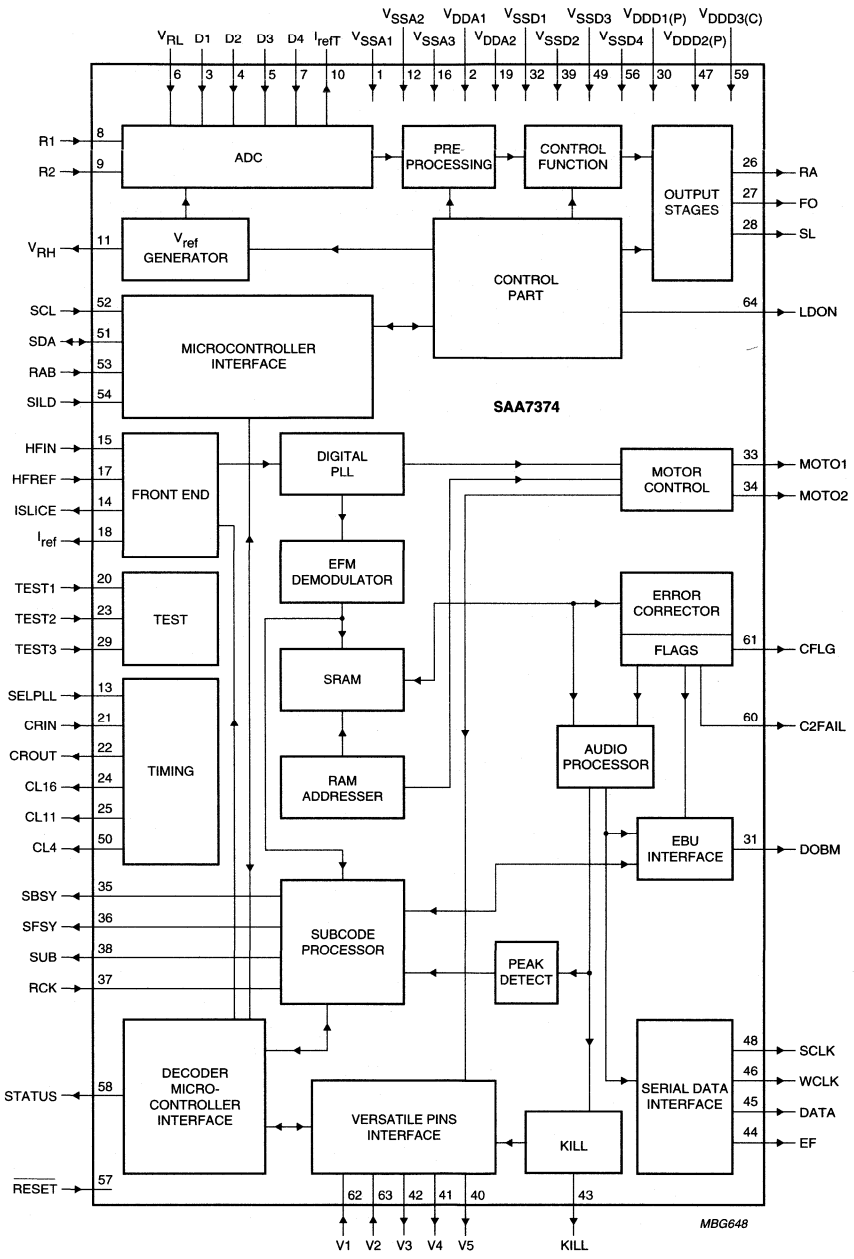


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSA1}	1[1]	analog ground 1
V_{DDA1}	2[1]	analog supply voltage 1
D1	3	unipolar current input (central diode signal input)
D2	4	unipolar current input (central diode signal input)
D3	5	unipolar current input (central diode signal input)
V_{RL}	6	reference voltage input for ADC
D4	7	unipolar current input (central diode signal input)
R1	8	unipolar current input (satellite diode signal input)
R2	9	unipolar current input (satellite diode signal input)
I_{refT}	10	current reference output for ADC calibration
V_{RH}	11	reference voltage output from ADC
V_{SSA2}	12[1]	analog ground 2
SELPLL	13	selects whether internal clock multiplier PLL is used
ISLICE	14	current feedback output from data slicer
HFIN	15	comparator signal input
V_{SSA3}	16[1]	analog ground 3
HFREF	17	comparator common mode input
I_{ref}	18	reference current output pin (nominally $0.5V_{DD}$)
V_{DDA2}	19[1]	analog supply voltage 2
TEST1	20	test control input 1; this pin should be tied LOW
CRIN	21	crystal/resonator input
CROUT	22	crystal/resonator output
TEST2	23	test control input 2; this pin should be tied LOW
CL16	24	16.9344 MHz system clock output
CL11	25	11.2896 or 5.6448MHz clock output (3-state)
RA	26	radial actuator output
FO	27	focus actuator output
SL	28	sledge control output
TEST3	29	test control input 3; this pin should be tied LOW
$V_{DDD1(P)}$	30[1]	digital supply voltage 1 for periphery
DOBM	31	bi-phase mark output (externally buffered; 3-state)
V_{SSD1}	32[1]	digital ground 1
MOTO1	33	motor output 1; versatile (3-state)
MOTO2	34	motor output 2; versatile (3-state)
SBSY	35	subcode block sync output (3-state)
SFSY	36	subcode frame sync output (3-state)
RCK	37	subcode clock input
SUB	38	P-to-W subcode bits output (3-state)
V_{SSD2}	39[1]	digital ground 2
V5	40	versatile output pin 5

SYMBOL	PIN	DESCRIPTION
V4	41	versatile output pin 4
V3	42	versatile output pin 3 (open-drain)
KILL	43	kill output (programmable; open-drain)
EF	44	C2 error flag; output only defined in CD ROM and $1f_s$ modes (3-state)
DATA	45	serial data output (3-state)
WCLK	46	word clock output (3-state)
$V_{DDD2(P)}$	47[1]	digital supply voltage 2 for periphery
SCLK	48	serial bit clock output (3-state)
V_{SSD3}	49[1]	digital ground 3
CL4	50	4.2336 MHz microcontroller clock output
SDA	51	microcontroller interface data I/O line (open-drain output)
SCL	52	microcontroller interface clock line input
RAB	53	microcontroller interface R/$\overline{W}$ and load control line input (4-wire bus mode)
SILD	54	microcontroller interface $\overline{R}$/W and load control line input (4-wire-bus mode)
n.c.	55	not connected
V_{SSD4}	56[1]	digital ground 4
$\overline{RESET}$	57	power-on reset input (active LOW)
STATUS	58	servo interrupt request line/decoder status register output (open-drain)
$V_{DDD3(C)}$	59[1]	digital supply voltage 3 for core
C2FAIL	60	indication of correction failure output (open-drain)
CFLG	61	correction flag output (open-drain)
V1	62	versatile input pin 1
V2	63	versatile input pin 2
LDON	64	laser drive on output (open-drain)

Note

1. All supply pins must be connected to the same external power supply voltage.

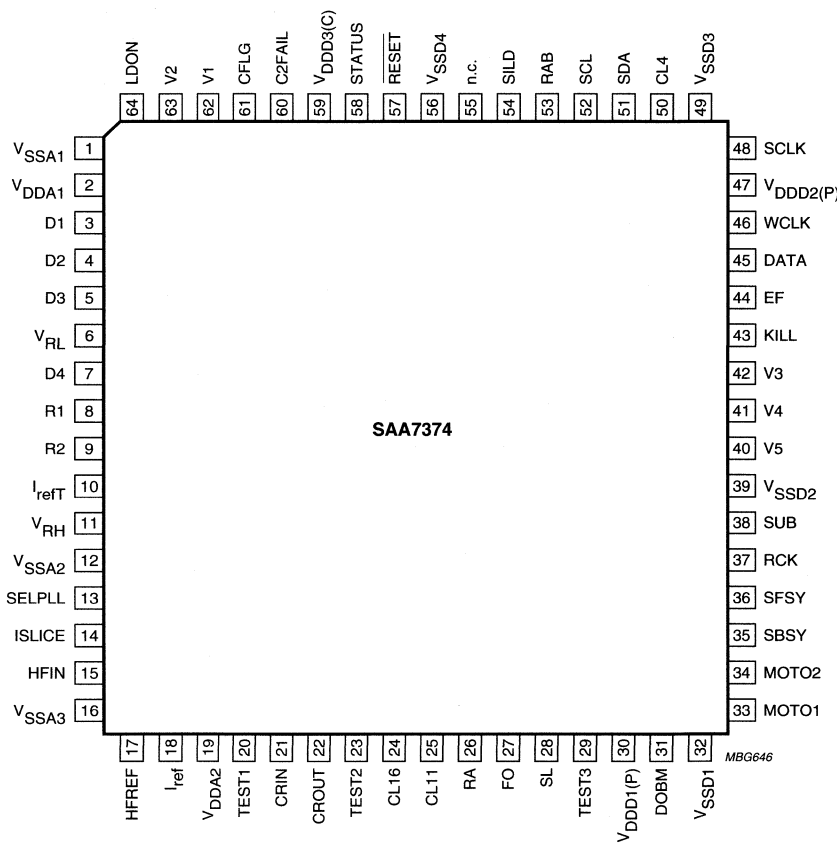


Fig.2 Pin configuration.

Digital servo processor and Compact Disc decoder (CD7)

SAA7376

CONTENTS

Digital servo processor and Compact Disc decoder (CD7)

SAA7376

1 FEATURES

- Single-speed mode
- Full error correction strategy, t = 2 and e = 4
- Full CD graphics interface
- All standard decoder functions implemented digitally on chip
- FIFO overflow concealment for rotational shock resistance
- Digital audio interface (EBU), audio only
- 2 and 4 times oversampling integrated digital filter, including f_s mode
- Audio data peak level detection
- Kill interface for DAC deactivation during digital silence
- All TDA1301 (DSIC2) digital servo functions, plus extra high-level functions
- Low focus noise
- Improved playability on ABEX TCD-721R, TCD-725 and TCD-714 discs
- Automatic closed loop gain control available for focus and radial loops
- Pulsed sledge support
- Microcontroller loading LOW
- High-level servo control option
- High-level mechanism monitor
- Communication may be via TDA1301/SAA7345 compatible bus or I^2C-bus
- On-chip clock multiplier allows the use of 8.4672 MHz crystal.

2 GENERAL DESCRIPTION

The SAA7376 is a single chip combining the functions of a CD decoder IC and digital servo IC. The decoder part is based on the SAA7345 (CD6) with an improved error correction strategy. The servo part is based on the TDA1301T (DSIC2) with improvements incorporated, extra features have also been added.

Supply of this Compact Disc IC does not convey an implied license under any patent right to use this IC in any Compact Disc application.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.4	5.0	5.5	V
I_{DD}	supply current		–	49	–	mA
f_{xtal}	crystal frequency		8	8.4672	35	MHz
T_{amb}	operating ambient temperature		−10	–	+70	°C
T_{stg}	storage temperature		−55	–	+125	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7376	QFP64	plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 × 14 × 2.7 mm	SOT393-1

5 BLOCK DIAGRAM

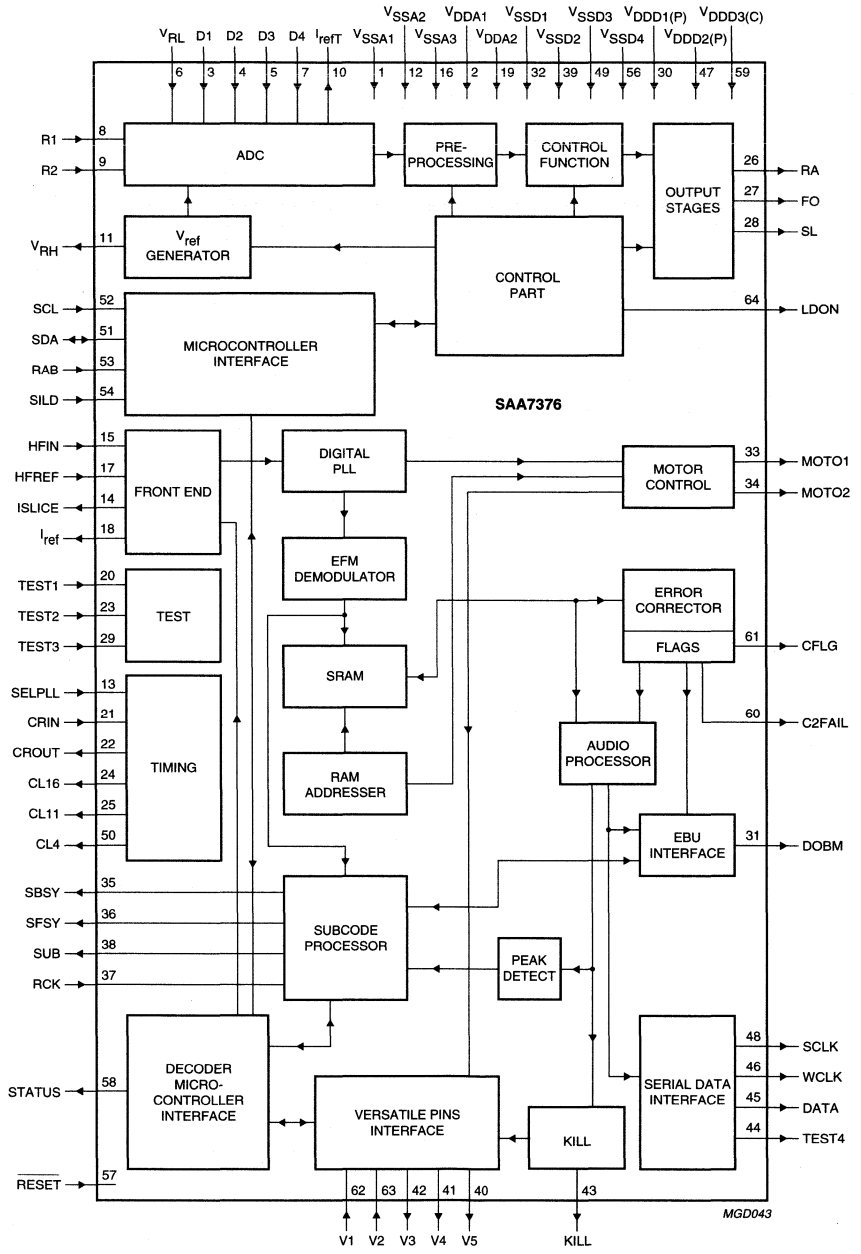


Fig.1 Block diagram.

6 PINNING

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V_{DDA2}	19[1]	analog supply voltage 2
TEST1	20	test control input 1; this pin should be tied LOW
CRIN	21	crystal/resonator input
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V3	42	versatile output pin 3 (open-drain)
KILL	43	kill output (programmable; open-drain)
TEST4	44	test output pin; this pin should be left unconnected
DATA	45	serial data output (3-state)
WCLK	46	word clock output (3-state)
$V_{DDD2(P)}$	47(1)	digital supply voltage 2 for periphery
SCLK	48	serial bit clock output (3-state)
V_{SSD3}	49(1)	digital ground 3
CL4	50	4.2336 MHz microcontroller clock output
SDA	51	microcontroller interface data I/O line (open-drain output)
SCL	52	microcontroller interface clock line input
RAB	53	microcontroller interface R/$\overline{W}$ and load control line input (4-wire bus mode)
SILD	54	microcontroller interface $\overline{R}$/W and load control line input (4-wire-bus mode)
n.c.	55	not connected
V_{SSD4}	56(1)	digital ground 4
$\overline{RESET}$	57	power-on reset input (active LOW)
STATUS	58	servo interrupt request line/decoder status register output (open-drain)
$V_{DDD3(C)}$	59(1)	digital supply voltage 3 for core
C2FAIL	60	indication of correction failure output (open-drain)
CFLG	61	correction flag output (open-drain)
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LDON	64	laser drive on output (open-drain)

Note

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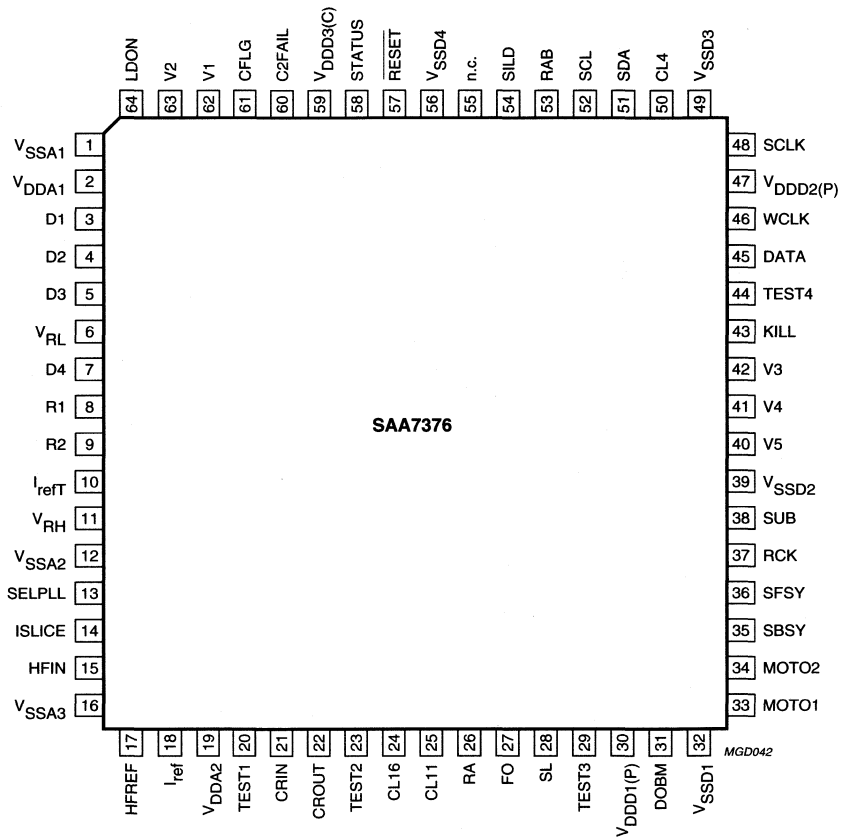


Fig.2 Pin configuration.

CONTENTS

1 FEATURES

- Supports real time error detection and correction in hardware. Error correction to n = 27, error detect to n = 30 and raw data transfer to n = 32.
- DVD-ROM supported in combination with the SAA7335
- Direct generic interface to external Small Computer Systems Interface (SCSI) controller devices
- Operates with up to 16 Mbytes DRAM
  - Hyper-page DRAM up to 33 Mbytes words/s burst
  - Fast-page DRAM at up to 17.5 Mbytes words/s burst
- Has fixed n = 1 or n = 2 rate (44.1 or 88.2 kHz) I^2S-bus multimedia output for simple audio/video output; features for CAV/quasi-CLV support
  - Supports Philips multimedia audio CODEC
  - Provides 'SHOARMA' Red Book audio buffer
- IEC 958 (SPDIF, AES/EBU and DOBM) output with Q-W subcode and programmable category code, output at n = 1 rate
- Device registers are memory mapped for faster direct access to the chip
- Provides direct access from sub-CPU to buffer RAM to support scratchpad accesses. This eliminates the need for extra RAM chips in the system
- Automatic sequencing of ATAPI packet command protocol, including command termination
- Automated data transfers to and from the host using PIO, DMA and ultra DMA.

2 GENERAL DESCRIPTION

The SAA7381 is a block decoder/encoder and buffer manager for high-speed CD-ROM/CD-R functions, that integrates real time error correction and detection and bidirectional ATAPI transfer functions into a single chip.

2.1 Memory mapped control registers

The SAA7381 device has a large number of memory mapped registers. These are arranged so that high-level languages see the registers as external byte or 16-bit integer quantities. The block addressing of the SAA7381 facilitates the use of pairs of 16-bit quantities to represent addresses.

The reading and writing of 16-bit registers within the device can be performed by two separate 8-bit reads, where the second byte data is latched at the same time as the first byte is read.

2.2 Error correction features

The SAA7381 has an on-chip 36 kbits memory that is used as a buffer memory for error and erasure correction processing. This buffer memory reduces the number of external RAM accesses that are needed for error correction and thus allows for an increased rate of data throughput.

The error corrector is switchable between two-pass, single-pass [both with Error Detection/Correction (EDC/ECC)] and EDC only modes to further improve throughput. The presence of the full error corrector removes the need for firmware based control of the error corrector's operation.

2.3 Host interface features

The SAA7381 has an ATAPI host interface that may be directly connected to the ATAPI bus thereby reducing the need for external support devices. It supports PIO Mode 4 transfer and Mode 0 ultra DMA. This interface can also be configured as a generic DMA interface for use with external host interface devices (e.g. SCSI controller). The DMA interface has the following features:

- ATAPI command packets are automatically loaded into the command FIFO
- Data transfer to the host is automatically sequenced to reduce inter-block latencies and improve host CPU utilisation
- Host data transfer rate is independent of error corrector operation and the data input path
- The host interface features automatic determination of block length for Mode 2, Form 1 and Form 2 sectors. The block length transferred is programmable.
- The host interface can transfer up to 3 sub-blocks per sector, with each sub-block being transferred dependent on the Form bit. Automatic reload of sub-block pointers and unconditional transfer are supported.

2.4 Buffer memory organisation

Memory is mapped as a 16-bit block number and 12-bit offset into that block. The block oriented memory structure permits the use of 16-bit pointers in software thereby minimising the overhead of accessing memory.
The address can be found from the following equation: address = block number × 2560 + offset.

The microcontroller sees the SAA7381 as a memory mapped peripheral, with control and status registers appearing in the upper address space.

The lowest 52 kbytes (48 kbytes + 4 kbytes) of the 8051 microcontroller external address space is mapped as a window into the memory on a user-specified 1 kbyte boundary within the buffer RAM. This can be used as a scratchpad memory.

The next 4 kbytes is separately mapped as a window into the memory on a user-specified 1 kbyte boundary within the RAM.

The next 7.5 kbytes of the external data space consists of three independently addressed memory segments for accessing block data, subcode information and block headers.

The registers of the SAA7381 are mapped into the top 256 bytes of external data space.

2.5 Subcode handling features

The writing of data into the buffer RAM is aligned to the absolute time sync marker with the following features:

- Subcodes are written into memory together with their associated sector data.This eases the provision of specialist features, for example CD + G or Karaoke CD applications.
- All channels of subcode are de-interleaved
- The Q channel is also Cyclic Redundancy Checked (CRC) for increased reliability
- When operating in 3-wire subcode mode, it is possible to control or read the P bit in the P-W subcode stream.

2.6 Multimedia output audio control features

The I²S-bus input may be processed before feeding to the multimedia audio output in several simple ways:

- As audio is transferred via the buffer memory, it is not necessary to have the CD-DSP I²S-bus input at exactly the audio n = 1 or video n = 2 rate. Any faster speed will work because the buffer RAM is used as a FIFO.
- Both channels may be independently controlled. The left channel output may be sourced from zero (digital silence), left or right input; this also applies for the right channel output. This permits basic audio switching and channel swapping.
- IEC 958 (SPDIF, AES/EBU and DOBM) output with Q-W subcode and programmable category code, can be output from the same CD-DSP I²S-bus data source.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{DDD(core)}$	digital core supply voltage	3.0	3.3	3.6	V
$V_{DDD(pad)}$	digital peripheral supply voltage	$V_{DDD(core)}$	5.0 or 3.3	5.0	V
I_{DDD}	supply current	tbf	60	tbf	mA
f_{xtal}	crystal frequency	8	8.4672, 11.289, 16.9344 or 33.8688	35	MHz
T_{amb}	operating ambient temperature	0	–	70	°C
T_{stg}	storage temperature	−55	–	+125	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7381	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1

5 BLOCK DIAGRAM

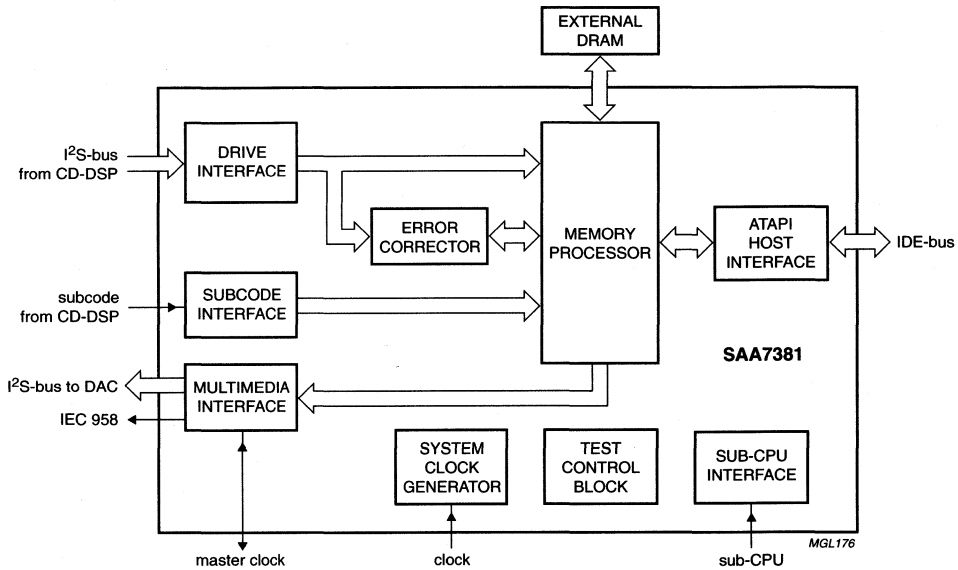


Fig.1 The SAA7381 internal block diagram.

6 PINNING

SYMBOL	PIN	TYPE	DRIVE/ THRESHOLD	GROUPING	DESCRIPTION
n.c.	1	–	–	–	not connected
n.c.	2	–	–	–	not connected
XDA0	3	O	M	RAM	output address lines
XDA1	4	O	M		
XDA2	5	O	M		
$V_{DDD(pad6)}$	6	–	–	–	digital peripheral supply voltage 6
DGND1	7	–	–	–	digital ground 1
XDA3	8	O	M	RAM	output address lines
XDA4	9	O	M		
XDA5	10	O	M		
XDA6	11	O	M		
XDA7	12	O	M		
XDA8	13	O	M		
XDA9	14	O	M		
XDA10	15	O	M		
XDA11	16	O	M		
DGND2	17	–	–	–	digital ground 2
$\overline{XRAS}$	18	O	H	RAM	row address strobe output (active LOW)
$\overline{XCAS}$	19	O	H		column address strobe output (active LOW)
$\overline{XWR}$	20	O	H		write enable output (active LOW)
XDD0	21	I/O	M/T	RAM	data bus input/output
XDD1	22	I/O	M/T		
$V_{DDD(core1)}$	23	–	–	–	digital core supply voltage 1
DGND3	24	–	–	–	digital ground 3
XDD2	25	I/O	M/T	RAM	data bus input/output
XDD3	26	I/O	M/T		
XDD4	27	I/O	M/T		
XDD5	28	I/O	M/T		
XDD6	29	I/O	M/T		
XDD7	30	I/O	M/T		
$V_{DDD(pad7)}$	31	–	–	–	digital peripheral supply voltage 7
DGND4	32	–	–	–	digital ground 4
SCKI1	33	I	C	I^2S-bus I/O	I^2S-bus bit clock input
WSI1	34	I	C		I^2S-bus word select strobe input

SYMBOL	PIN	TYPE	DRIVE/ THRESHOLD	GROUPING	DESCRIPTION
n.c.	35 to 38	–	–	–	not connected
SDI1	39	I	C	I^2S-bus I/O	data input from CD engine
n.c.	40	O	M		not connected
SFSY	41	I/O	L/C	subcode I/O	3-wire subcode sync input/output
RCK	42	I/O	L/C		3-wire subcode clock input/output
SUBI	43	I	C		Q and R-W subcode input
n.c.	44	O	L		not connected
CFLG	45	I	C	I^2S-bus input	CD error corrector flags and absolute time sync
C2P0	46	I	C		CD C2 error correction flag input for ERCO
DGND5	47	–	–	–	digital ground 5
IECO	48	O	M	multimedia	IEC 958 output
MCK	49	I/O	M/C	multimedia output	$256f_s$ or $384f_s$ clock for multimedia master clock/IEC 958 clock or divided system clock for CD-DSP
SCK2	50	I/O	L/C	multimedia	I^2S-bus bit clock input/output
WS2	51	I/O	L/C		I^2S-bus word select strobe input/output
SDO2	52	O	M		I^2S-bus data output to DAC/video decoder
GND	53	–	–	–	ground
CROUT	54	O	crystal pad	crystal oscillator	crystal oscillator output
CRIN	55	I	crystal pad		crystal oscillator/clock input
V_{DDA}	56	–	–	–	analog supply voltage
I_{ref}	57	analog	current input	clock generator	VCO reference current
$\overline{POR}$	58	I	Schmitt trigger	system	power-on reset (active LOW)
TEST1	59	I	C	test	mode control input test pins
TEST2	60	I	C		
$\overline{RESET}$	61	I	Schmitt trigger	host	ATAPI bus reset input from host (active LOW)
DD7	62	I/O	AL/T	host	data bus input/output
DD8	63	I/O	AL/T		
DD6	64	I/O	AL/T		
$V_{DDD(pad1)}$	65	–	–	–	digital peripheral supply voltage 1
DGND6	66	–	–	–	digital ground 6
DD9	67	I/O	AL/T	host	data bus pin order of ATAPI interface matches the pinning of the 40-way IDE connector (slew rate limiting by control of drive capability into capacitive load of ATA bus)
DD5	68	I/O	AL/T		
DD10	69	I/O	AL/T		
DD4	70	I/O	AL/T		

SYMBOL	PIN	TYPE	DRIVE/ THRESHOLD	GROUPING	DESCRIPTION
n.c.	71 to 74	–	–	–	not connected
DD11	75	I/O	AL/T	host	data bus; pin order of ATAPI interface matches the pinning of the 40-way IDE connector (slew rate limiting by control of drive capability into capacitive load of ATA bus)
DD3	76	I/O	AL/T		
DD12	77	I/O	AL/T		
DD2	78	I/O	AL/T		
DD13	79	I/O	AL/T		
DD1	80	I/O	AL/T		
DD14	81	I/O	AL/T		
DD0	82	I/O	AL/T		
DD15	83	I/O	AL/T		
DMARQ/ $\overline{\text{DMACK}}$	84	O	AL	host	DMA request/SCSI DMA acknowledge output (active LOW)
DGND7	85	–	–	–	digital ground 7
$V_{DDD(pad2)}$	86	–	–	–	digital peripheral supply voltage 2
$\overline{\text{DIOW}}$	87	I	L/T	host	write cycle write enable/control register write input (active LOW)
$\overline{\text{DIOR}}$	88	I	L/T	host	read cycle read enable/control register read input (active LOW)
$\overline{\text{IORDY}}$	89	O	AH	host	device is ready to transfer data output (active LOW)
$\overline{\text{DMACK}}$/ DMARQ	90	I	T	host	DMA acknowledge (active LOW)/SCSI DMA request input
INTRQ	91		A	host	host interrupt request (NB 3-state output)
DGND8	92	–	–	–	digital ground 8
$V_{DDD(pad3)}$	93	–	–	–	digital peripheral supply voltage 3
$\overline{\text{IOCS16}}$	94	O	AH	host	I/O port is 16-bit output (active LOW)
DA1/$\overline{\text{DBWR}}$	95	I/O	L/T	host	address wire 1/DMA from generic interface is output from the SAA7381 (active LOW)
$\overline{\text{PDIAG}}$	96	I/O	AL/T	host	ATAPI passed diagnostics input/output (active LOW)
DA0	97	I/O	L/T	host	address wire 0 input/output
DA2/$\overline{\text{DBRD}}$	98	I/O	L/T	host	address wire 2/DMA from generic interface is input to the SAA7381 (active LOW)
$\overline{\text{CS0}}$/ $\overline{\text{SCSICS}}$	99	I/O	L/T	host	chip select 1FX/generic interface chip select (active LOW)
$\overline{\text{CS1}}$	100	I/O	L/T	host	chip select 3FX input/output (active LOW)
$\overline{\text{DASP}}$	101	I/O	AH/T	host	device active slave present input/output (active LOW)
INT2	102	O	L	sub-CPU	sub-CPU interrupt output from the SAA7381 drive block and UART

SYMBOL	PIN	TYPE	DRIVE/ THRESHOLD	GROUPING	DESCRIPTION
DGND9	103	–	–	–	digital ground 9
$V_{DDD(pad4)}$	104	–	–	–	digital peripheral supply voltage 4
COMACK	105	I	C	UART	command acknowledge/transmit flow control input
COMCLK	106	O	L	UART	serial data clock for synchronous mode output
n.c.	107 to 110	–	–	–	not connected
COMOUT	111	O	L	UART	transmit data output
COMIN	112	I	C	UART	receive data input
COMSYNC	113	I	C	UART	basic engine synchronization input
SYSSYNC	114	I	C	UART	basic engine synchronization input
SCCLK	115	O	M	sub-CPU	sub-CPU clock output
$\overline{RD}$	116	I	T	sub-CPU	sub-CPU read enable (active LOW)
$\overline{WR}$/R/$\overline{W}$	117	I	T	sub-CPU	sub-CPU write enable/and read/write control input (active LOW)
$\overline{INT}$	118	O	L	sub-CPU	sub-CPU interrupt request output from host interface (active LOW)
SRST	119	O	L	sub-CPU	sub-CPU reset output
SCA0/SCD0	120	I/O	L/T	sub-CPU	multiplexed address/data lines
SCA1/SCD1	121	I/O	L/T		
DGND10	122	–	–	–	digital ground 10
$V_{DDD(pad5)}$	123	–	–	–	digital peripheral supply voltage 6
SCA2/SCD2	124	I/O	L/T	sub-CPU	multiplexed address/data lines
SCA3/SCD3	125	I/O	L/T		
SCA4/SCD4	126	I/O	L/T		
SCA5/SCD5	127	I/O	L/T		
SCA6/SCD6	128	I/O	L/T		
SCA7/SCD7	129	I/O	L/T		
DGND11	130	–	–	–	digital ground 11
$V_{DDD(core2)}$	131	–	–	–	digital core supply voltage 2
ALE	132	I	T	sub-CPU	demultiplex enable input for lower address lines
$\overline{PSEN}$	133	I	T	sub-CPU	program store enable (active LOW)
SCA15	134	I	T	sub-CPU	upper address lines input
SCA14	135	I	T		
SCA13	136	I	T		
SCA12	137	I	T		
DGND12	138	–	–	–	digital ground 12

SYMBOL	PIN	TYPE	DRIVE/ THRESHOLD	GROUPING	DESCRIPTION
SCA11	139	I	T	sub-CPU	upper address lines input
SCA10	140	I	T		
SCA9	141	I	T		
SCA8	142	I	T		
n.c.	143	–	–	–	not connected
n.c.	144	–	–	–	not connected

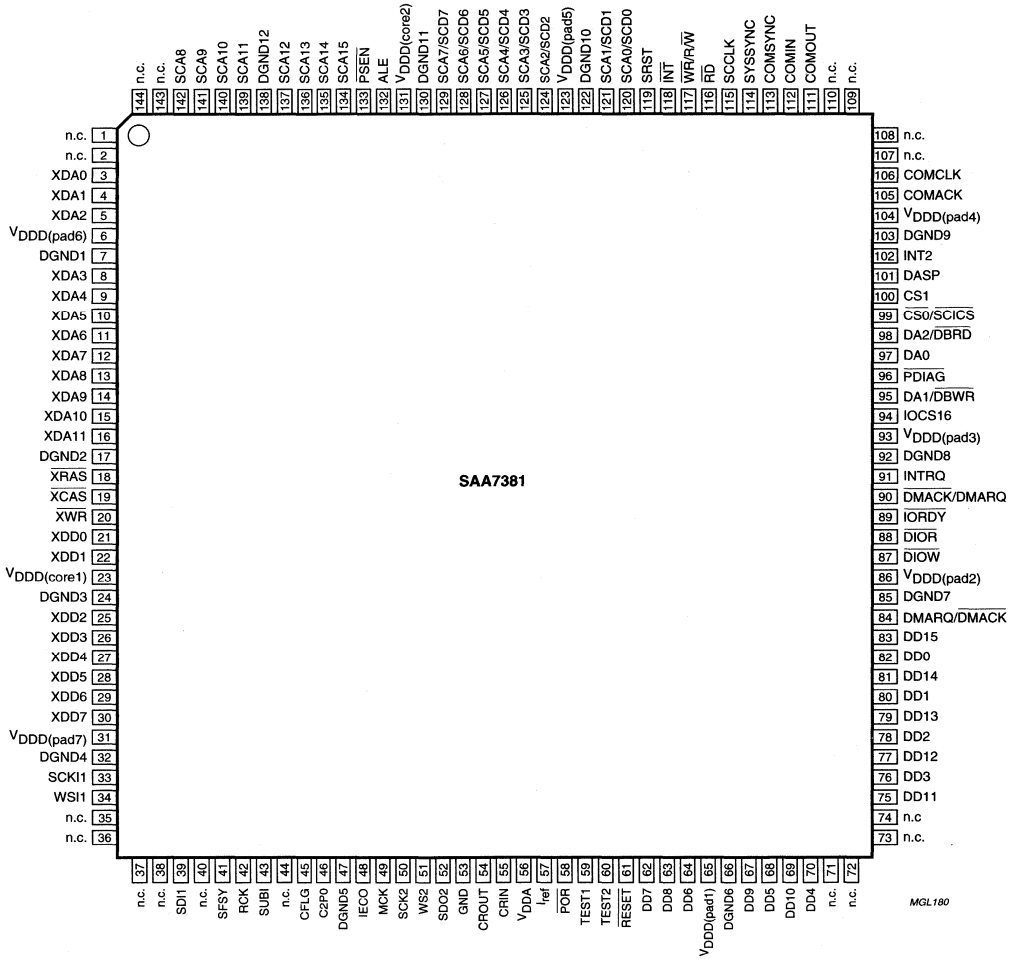


Fig.2 Pin configuration.

6.1 Detailed description of pin functions

Table 1 Q and R-W input/output subcode connections (4 pins)

SYMBOL	DESCRIPTION	COMMENT
SFSY	3-wire subcode sync	input subcode frame sync for receiving 3-wire subcode; output subcode frame sync for transmitting 3-wire subcode
RCK	3-wire subcode clock	output bit clock for receiving 3-wire subcode; input bit clock for transmitting 3-wire subcode
SUBI	Q and R-W subcode input	configurable for 3-wire or Philips V4 subcode mode; can use either RCK or WSI1 as clock references with appropriate dividers

Table 2 I^2S-bus multimedia audio output (5 pins)

SYMBOL	DESCRIPTION	COMMENT
MCK	$256f_s$ or $384f_s$ clock for multimedia master clock/IEC 958 clock or divided system clock for CD-DSP	Clock reference input pin when interface is in a master mode; a programmable divider is provided. This pin is also configurable as a programmable clock output intended as a clock reference for a CD-DSP. Should be pulled up if not in use.
SCK2	I^2S-bus bit clock	This is used for master and slave I^2S-bus application as both modes are needed. For instance, the Philips multimedia CODEC is an I^2S-bus slave, hence this must be a master interface. When driving some DACs, this interface can be a slave.
WS2	I^2S-bus left/right strobe	word select strobe either master or slave
SDO2	I^2S-bus data to DAC/video decoder	I^2S-bus multimedia data
IECO	IEC 958 output	the IEC 958 output combines multimedia data and Q-W subcode

Table 3 I^2S-bus connections to CD engine (6 pins)

SYMBOL	DESCRIPTION	COMMENT
SCKI1	I^2S-bus bit clock	this is a separate clock to the multimedia bit clock as this rate is derived from the disc linear velocity
WSI1	I^2S-bus left/right strobe	
SDI1	I^2S-bus data from CD-DSP	
C2P0	CD C2 error corrector flag from ERCO	these flags are used to indicate errors from second layer correction to the ERCO
CFLG	CD error corrector flags and absolute time sync	The absolute time sync is used in the CD input process for playing 'Red Book' discs; the error corrector status is also read in from this signal, to provide an indication of C1 and C2 performance for CD-RW applications.

Table 4 ATAPI target mode interface

ATAPI NAME	ATAPI MEANING
$\overline{\text{RESET}}$	ATAPI reset signal: the SAA7381 will not recognize a signal assertion shorter than 20 ns as a valid reset signal.
DD0 to DD7	ATAPI D0 to D7.
DD8 to DD15	ATAPI D8 to D15: these data bits are only used in accesses to the 16-bit data port.
DMARQ	DMA request: this signal, used for DMA data transfers between host and device, is asserted by the SAA7381 when it is ready to transfer data to or from the host. The direction of data transfer is controlled by $\overline{\text{DIOR}}$ and $\overline{\text{DIOW}}$.
$\overline{\text{DMACK}}$	DMA acknowledge: this signal is used by the host in response to DMARQ to initiate DMA transfers. This signal may be temporarily negated by the host to suspend the DMA transfer in process.
$\overline{\text{IOCS16}}$	ATAPI I/O port is a 16-bit open-drain output: during PIO transfer Modes 0, 1 or 2, $\overline{\text{IOCS16}}$ indicates to the host system that the 16-bit data port has been addressed and that the device is prepared to send or receive a 16-bit data word.
$\overline{\text{IORDY}}$	ATAPI I/O ready open-drain output: this signal is negated to extend the host transfer cycle of any host register access (read or write) when the SAA7381 is not ready to respond to a data transfer request. This signal is only enabled during $\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ cycles to the SAA7381. When $\overline{\text{IORDY}}$ is not active, it is in the high-impedance (undriven) state.
DA0 to DA2	Address bus (device address).
$\overline{\text{DIOW}}$	ATAPI write strobe: the rising edge of $\overline{\text{DIOW}}$ latches data from the signals, DD0 to DD7 or DD0 to DD15 into a register or the data port of the SAA7381. The SAA7381 will not act on the data until it is latched.
$\overline{\text{DIOR}}$	ATAPI read strobe: the falling edge of $\overline{\text{DIOR}}$ enables data from a register or data port of the SAA7381 onto the signals, DD0 to DD7 or DD0 to DD15. The rising edge of $\overline{\text{DIOR}}$ latches data at the host and the host will not act on the data until it is latched.
$\overline{\text{CS0}}$	ATAPI chip select 0 input: this is the chip select signal from the host used to select the ATA command block registers. This signal is also known as $\overline{\text{CS1FX}}$.
$\overline{\text{CS1}}$	ATAPI chip select 1 input: this is the chip select signal from the host used to select the ATA control block registers. This signal is also known as $\overline{\text{CS3FX}}$.
INTRQ	ATAPI interrupt output: this signal is used to interrupt the host system. INTRQ is asserted only when the device has a pending interrupt, the device is selected, and the host has cleared the 'nien' bit in the device control register. If the 'nien' bit is equal to 1, or the device is not selected, this output is in a high-impedance state, regardless of the presence or absence of a pending interrupt.
$\overline{\text{PDIAG}}$	ATAPI passed diagnostics: this signal shall be asserted by device 1 to indicate to device 0 that it has completed diagnostics.
$\overline{\text{DASP}}$	ATAPI DASP (device active, device 1 present): this is a time-multiplexed signal which indicates that a device is active, or that device 1 is present. This signal is an open-drain output.

Table 5 Generic host controller interface

ATAPI NAME	GENERIC INTERFACE NAME	GENERIC HOST CONTROLLER INTERFACE MEANING
$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	controller reset output
DD0 to DD7	D0 to D7	controller DMA path/controller data and control bus (optional)
DD8 to DD15	D8 to D15	controller upper DMA path (optional)
DMARQ	$\overline{\text{DMACK}}$	DMA acknowledge to controller
$\overline{\text{DMACK}}$	DMARQ	DMA request from controller
DA1	$\overline{\text{DBWR}}$	DMA bus write to controller
DA2	$\overline{\text{DBRD}}$	DMA bus read from controller
$\overline{\text{CS0}}$	$\overline{\text{SCSICS}}$	controller chip select output for sub-CPU read/write cycles

Table 6 Miscellaneous pins

SYMBOL	DESCRIPTION	COMMENT
CRIN	crystal oscillator/clock input	–
CROUT	crystal oscillator output	–
I_{ref}	VCO reference current	clock PLL multiplier
$\overline{\text{POR}}$	power-on reset pin	–
TEST1 and TEST2	mode control test pins	–

Table 7 Sub-CPU interface pins

SYMBOL	DESCRIPTION	COMMENT
SRST	sub-CPU reset	active HIGH reset if XDD7 is pulled LOW during power-on reset; active LOW reset if XDD7 is pulled HIGH during power-on reset
$\overline{\text{INT}}$	sub-CPU interrupt request output from host interface	open-drain sub-processor interrupt from host interface
INT2	sub-CPU interrupt output from the SAA7381 drive block and UART	open-drain sub-processor interrupt from drive and UART
SCCLK	sub-CPU clock out	–
$\overline{\text{RD}}$	sub-CPU read enable	sub-CPU read enable strobe; if grounded permanently, the $\overline{\text{WR}}$ signal will act as read/write control input
$\overline{\text{WR}}$/R/$\overline{\text{W}}$	sub-CPU write enable/ read/write control	write enable; alternative usage is read/$\overline{\text{write}}$ if $\overline{\text{RD}}$ is held LOW at all times; $\overline{\text{WR}}$ has priority over $\overline{\text{RD}}$ at all times
ALE	demultiplex enable input for lower address lines	while HIGH, the lower address bits are latched from SCD0 to SCD7; should be used with a Schmitt trigger input to avoid false latching due to ground bounce on the 8051 microcontroller
$\overline{\text{PSEN}}$	program store enable	this pin should be tied high using a 10 kΩ resistor
SCD0 to SCD7/ SCA0 to SCA7	sub-CPU data bus multiplexed/low address bus	–
SCA8 to SCA15	sub-CPU address high bits	–

Table 8 RAM interface pins

SYMBOL	DESCRIPTION	COMMENT
XDA0 to XDA11	RAM address bits, multiplexed for DRAM	up to 16 Mbytes DRAM only supported
$\overline{\text{XRAS}}$	DRAM row address strobe	
$\overline{\text{XCAS}}$	DRAM column address strobe	
$\overline{\text{XWR}}$	RAM write enable	
XDD0 to XDD7	RAM data bus	

Table 9 Basic engine interface

SYMBOL	DESCRIPTION	COMMENT
SYSSYNC	basic engine synchronization input	generate interrupts on rising and/or falling edges
COMSYNC	basic engine synchronization input	generate interrupts on rising and/or falling edges
COMIN	receive data	–
COMOUT	transmit data	–
COMCLK	serial data clock for synchronous mode	–
COMACK	command acknowledge/transmit flow control	must be HIGH for synchronous mode to transmit next data byte

Error correction and host interface IC for CD-ROM (SEQUOIA)

SAA7385

CONTENTS

Error correction and host interface IC for CD-ROM (SEQUOIA) SAA7385

1 FEATURES

1.1 General

- Single chip digital solution for an 8 × speed CD-ROM controller chip
- 10 Mbytes/s NCR53CF94 equivalent SCSI controller included
- High-speed 80C32 microcontroller with 256 × 8 scratch-pad SRAM included
- High performance CD-ROM interface logic
- 128 pin QFP package.

1.2 53CF94 SCSI controller

- Separate clock input to allow operation up to the maximum 10 Mbytes/s
- Fast synchronous SCSI-2 compatible
- 24-bit transfer counter for single transfers up to 16 Mbytes
- High-speed 16-bit DMA interface to the buffer manager DRAM
- On-chip 48 mA SCSI drivers
- Software compatible with members of the 53C90 family
- Allows for SCAM support.

1.3 80C32 high-speed microcontroller

- 33.87 MHz full system speed operation
- Three timers/event counters
- Programmable full duplex serial channel
- Eight general purpose microcontroller I/O pins
- External program ROM.

1.4 Front-end interface logic

- Full 8 × speed hardware operation
- Block decoder
- Sector sequencer
- CRC checking of Mode 1 and Mode 2, Form 1 sectors
- 212 ms watch-dog timer
- Sub-code interface with synchronization
- C-flag interface for absolute time stamp.

1.5 Buffer controller

- Ten level arbitration logic
- Utilizes low cost 70 ns DRAMs
- Page mode DRAM access for high-speed error correction and SCSI data transfer
- Data organization by 3 kbyte frames
- 256 kbyte or 1 Mbyte DRAM supported.

1.6 Hardware third-level error correction

- Third-level correction provides superior performance in unfavourable conditions
- Full hardware error correction to reduce microcontroller overhead
- Corrections are automatically written to the DRAM frame buffer.

1.7 Additional product support

- All control registers mapped into 80C32 special function memory space
- Dedicated S2B interface UART
- Input clock synthesizer
- Red book audio pass through.

2 GENERAL DESCRIPTION

The SAA7385 is a high integration ASIC that incorporates all of the digital electronics necessary to connect a CD decoder to a SCSI host. An 80C32 microcontroller and a 53CF94 SCSI controller are embedded in the ASIC. The following functions are supported:

- Input clock doubler
- Block decoder
- CRC checking of Mode 1 and Mode 2, Form 1 sectors
- Red book audio pass through to SCSI
- Buffer manager
- Third-level error correction
- Sub-code and Q-channel support
- Dedicated S2B interface UART
- Embedded 80C32 microcontroller
- Embedded 53CF94 SCSI controller.

The SAA7385 uses a 33.8688 MHz clock and is capable of accepting data at eight times (n = 8 or 1.4 Mbytes/s) the normal CD-ROM data rate.

Third level error correction hardware is included to improve the correction efficiency of the system. The buffer manager hardware utilizes a ten-level arbitration unit and can stop the clock to the microcontroller to emulate a wait condition when necessary.

The SAA7385 comprises five major functional blocks:

- The 80C32 microcontroller is an industry standard core
- The 53CF94 is an industry standard core
- The front-end block connects to the external CD-60 based decoder and fully processes the incoming data stream to provide bytes of data that are stored in the external buffer
- The buffer manager block provides the address generation and timing control for the external DRAM buffer
- The ECC block performs the error correction functions in hardware on the data in the DRAM buffer.

Supply of this Compact Disc IC does not convey an implied license under any patent right to use this IC in any Compact Disc application.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	digital supply voltage	4.5	5.0	5.5	V
T_{amb}	operating ambient temperature	0	–	70	°C
T_{stg}	storage temperature	−55	–	+150	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7385GP	SQFP128	plastic quad flat package; 128 leads (lead length 1.6 mm); body 14 × 20 × 2.8 mm	SOT387-2

5 BLOCK DIAGRAM

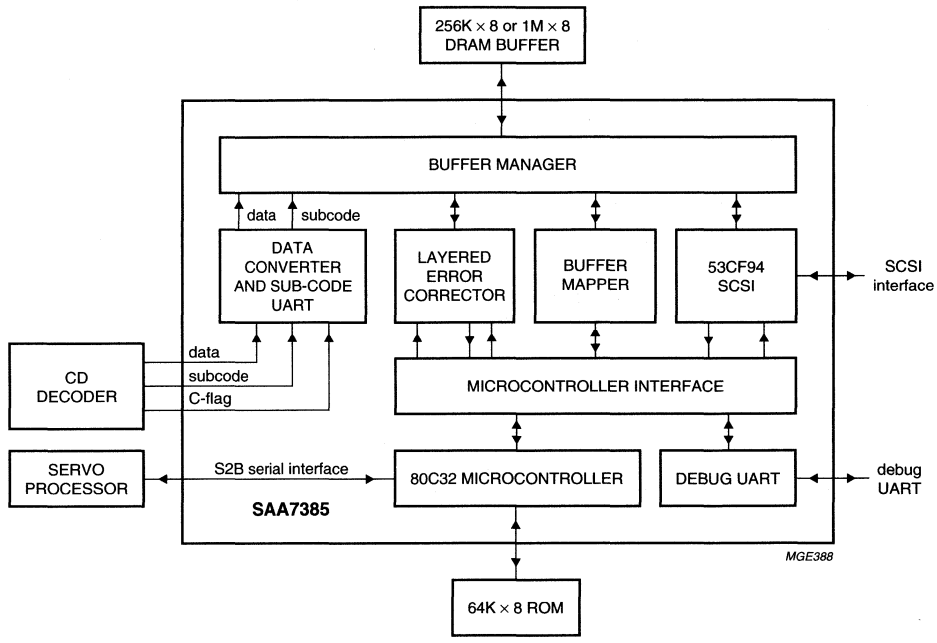


Fig.1 Block diagram (simplified).

6 PINNING

All input, output and bidirectional signals are TTL level unless otherwise stated (Pull-Down = PD25 = 25 μA; Pull-Up = PU25 = 25 μA, PU400 = 400 μA; Slew = S2 = 2 mA, S4 = 4 mA; CMOS slew = CMOS S2 = CMOS 2 = 2 mA; SCSI pad = SCSI = 48 mA).

SYMBOL	PIN	I/O	PAD	DESCRIPTION
DA2	1	O	S4	DRAM address bus; bit DA2
DA3	2	O	S4	DRAM address bus; bit DA3
DA4	3	O	S4	DRAM address bus; bit DA4
V_{SS1}	4	–	–	ground 1
DA5	5	O	S4	DRAM address bus; bit DA5
DA6	6	O	S4	DRAM address bus; bit DA6
DA7	7	O	S4	DRAM address bus; bit DA7
DA8	8	O	S4	DRAM address bus; bit DA8
DA9	9	O	S4	DRAM address bus; bit DA9
V_{DD1}	10	–	–	power supply 1

SYMBOL	PIN	I/O	PAD	DESCRIPTION
$\overline{RAS}$	11	O	S4	DRAM row address section; active LOW
$\overline{CAS}$	12	O	S4	DRAM column address selection; active LOW
$\overline{DWR}$	13	O	S4	DRAM write; active LOW
$\overline{DOE}$	14	O	S4	DRAM output enable; active LOW
V_{SS2}	15	–	–	ground 2
DD0	16	I/O	4 mA, Schmitt, PD25	DRAM data bus; bit DD0
DD1	17	I/O	4 mA, Schmitt, PD25	DRAM data bus; bit DD1
DD2	18	I/O	4 mA, Schmitt, PD25	DRAM data bus; bit DD2
DD3	19	I/O	4 mA, Schmitt, PD25	DRAM data bus; bit DD3
V_{DD2}	20	–	–	power supply 2
DD4	21	I/O	4 mA, Schmitt, PD25	DRAM data bus; bit DD4
DD5	22	I/O	4 mA, Schmitt, PD25	DRAM data bus; bit DD5
DD6	23	I/O	4 mA, Schmitt, PD25	DRAM data bus; bit DD6
DD7	24	I/O	4 mA, Schmitt, PD25	DRAM data bus; bit DD7
V_{SS3}	25	–	–	ground 3
$\overline{LED}$	26	O	24 mA, CMOS test	panel LED; active LOW; WTGCTL(4)
$\overline{TRAYSW}$	27	I	Schmitt, PU25	active LOW when tray is in
$\overline{EJECT}$	28	I	Schmitt, PU25	opens tray; active LOW
LQDATA	29	O	2 mA	serial data to DAC
LWCLK	30	O	2 mA	word strobe to DAC
V_{SS4}	31	–	–	ground 4
SCLK	32	O	2 mA	data serial clock
V_{SS5}	33	–	–	ground 5
SYSRES	34	O	2 mA, PU25	system reset; OR of $\overline{POR}$, $\overline{SCSIRST}$ and watch-dog timer
CFLAG	35	I	Schmitt, PU400	C1 and C2 status
$\overline{CPR}$	36	O	2 mA	S2B interface ready to accept data; active LOW
$\overline{SPR}$	37	I	Schmitt	S2B interface ready to send data; active LOW
$\overline{SKIPFWD}$	38	I	Schmitt, PU25	skip forwards; active LOW; RDSW(3)
$\overline{SKIPBACK}$	39	I	Schmitt, PU25	skip backwards; active LOW; RDSW(2)
SCSICLK	40	I	standard	SCSI interface clock
V_{DD3}	41	–	–	power supply 3
AD0	42	I/O	S4, Schmitt	microcontroller multiplexed data bus; bit AD0
AD1	43	I/O	S4, Schmitt	microcontroller multiplexed data bus; bit AD1
AD2	44	I/O	S4, Schmitt	microcontroller multiplexed data bus; bit AD2
AD3	45	I/O	S4, Schmitt	microcontroller multiplexed data bus; bit AD3
AD4	46	I/O	S4, Schmitt	microcontroller multiplexed data bus; bit AD4
AD5	47	I/O	S4, Schmitt	microcontroller multiplexed data bus; bit AD5
AD6	48	I/O	S4, Schmitt	microcontroller multiplexed data bus; bit AD6
AD7	49	I/O	S4, Schmitt	microcontroller multiplexed data bus; bit AD7
V_{SS6}	50	–	–	ground 6
LA0	51	O	CMOS S2, PU25	EPROM latched lower address; bit LA0

SYMBOL	PIN	I/O	PAD	DESCRIPTION
LA1	52	O	CMOS S2, PU25	EPROM latched lower address; bit LA1
LA2	53	O	CMOS S2, PU25	EPROM latched lower address; bit LA2
LA3	54	O	CMOS S2, PU25	EPROM latched lower address; bit LA3
V_{DD4}	55	–	–	power supply 4
LA4	56	O	CMOS S2, PU25	EPROM latched lower address; bit LA4
LA5	57	O	CMOS S2, PU25	EPROM latched lower address; bit LA5
LA6	58	O	CMOS S2, PU25	EPROM latched lower address; bit LA6
LA7	59	O	CMOS S2, PU25	EPROM latched lower address; bit LA7
V_{SS7}	60	–	–	ground 7
A8	61	O	CMOS S2, PU25	EPROM upper address; bit A8
A9	62	O	CMOS S2, PU25	EPROM upper address; bit A9
A10	63	O	CMOS S2, PU25	EPROM upper address; bit A10
A11	64	O	CMOS S2, PU25	EPROM upper address; bit A11
A12	65	O	CMOS S2, PU25	EPROM upper address; bit A12
A13	66	O	CMOS S2, PU25	EPROM upper address; bit A13
A14	67	O	CMOS S2, PU25	EPROM upper address; bit A14
A15	68	O	CMOS S2, PU25	EPROM upper address; bit A15
$\overline{PSEN}$	69	O	CMOS 2, PU25	program store enable; active LOW
V_{SS8}	70	–	–	ground 8
$\overline{IO}$	71	I/O	SCSI	SCSI phase signal, active LOW
$\overline{REQ}$	72	I/O	SCSI	SCSI request, active LOW
$\overline{CD}$	73	I/O	SCSI	SCSI phase signal, active LOW
$\overline{SEL}$	74	I/O	SCSI	SCSI select, active LOW
V_{SS9}	75	–	–	ground 9
$\overline{MSG}$	76	I/O	SCSI	SCSI phase signal, active LOW
$\overline{ACK}$	77	I/O	SCSI	SCSI acknowledge, active LOW
$\overline{BSY}$	78	I/O	SCSI	SCSI busy, active LOW
V_{SS10}	79	–	–	ground 10
$\overline{ATN}$	80	I/O	SCSI	output in initiator mode; input in target mode, active LOW
V_{DD5}	81	–	–	power supply 5
$\overline{SDP}$	82	I/O	SCSI	SCSI parity, active LOW
SD7	83	I/O	SCSI	SCSI data bus; bit SD7
SD6	84	I/O	SCSI	SCSI data bus; bit SD6
SD5	85	I/O	SCSI	SCSI data bus; bit SD5
V_{SS11}	86	–	–	ground 11
SD4	87	I/O	SCSI	SCSI data bus; bit SD4
SD3	88	I/O	SCSI	SCSI data bus; bit SD3
SD2	89	I/O	SCSI	SCSI data bus; bit SD2
SD1	90	I/O	SCSI	SCSI data bus; bit SD1
SD0	91	I/O	SCSI	SCSI data bus; bit SD0
V_{SS12}	92	–	–	ground 12

SYMBOL	PIN	I/O	PAD	DESCRIPTION
RXS2B	93	I	Schmitt, PU25	S2B interface receive
TXS2B	94	O	4 mA	S2B interface transmit
$\overline{\text{TRAYIN}}$	95	I/O	4 mA, PD25	tray extend control; active LOW (general purpose signal)
$\overline{\text{TRAYOUT}}$	96	I/O	4 mA, PD25	tray retract control; active LOW (general purpose signal)
$\overline{\text{SCSIRST}}$	97	I	Schmitt	SCSI reset, active LOW; also causes a system reset
$\overline{\text{POR}}$	98	I	CMOS	power-on reset; active LOW
V_{DD6}	99	–	–	power supply 6
UC_PORT1.7	100	I/O	CMOS 2, PU25	drive speed select; microcontroller port 1.7
RAB_MUSB	101	I/O	CMOS 2, PU25	RD/WR, acknowledge; microcontroller port 1.2
NRST_SEQ	102	I/O	CMOS 2, PU25	reset to engine; microcontroller port 1.5
UC_PORT1.4	103	I/O	CMOS 2, PU25	general purpose microcontroller I/O port; port 1.4
UC_PORT1.3	104	I/O	CMOS 2, PU25	general purpose microcontroller I/O port; port 1.3
UC_PORT1.1	105	I/O	CMOS 2, PU25	general purpose microcontroller I/O port; port 1.1
$\overline{\text{HOMESW}}$	106	I/O	2 mA, PU25	actuator sled home; active LOW; microcontroller port 1.0
$\overline{\text{PLAY}}$	107	I	Schmitt	laser on and focused status; active LOW; RDSW(4)
UC_PORT1.6	108	I/O	CMOS 2, PU25	general purpose microcontroller I/O port; port 1.6
V_{SS13}	109	–	–	ground 13
GPI1	110	I	Schmitt, PU25	general purpose input; microcontroller port 3.4
GPI2	111	I	Schmitt, PU25	general purpose input; microcontroller port 3.5
$\overline{\text{KILL}}$	112	I	Schmitt, PU25	shut off audio; active LOW
TXICE	113	O	4 mA	debug UART output; from 80C32 serial port
RXICE	114	I	Schmitt, PU25	debug UART input; to 80C32 serial port
RXSUB	115	I	Schmitt, PU25	sub-code input
V_{DD7}	116	–	–	power supply 7
OSCIN	117	I	standard	master input clock; 34 or 16 MHz
V_{SS14}	118	–	–	ground 14
CLAB	119	I	Schmitt	clock
V_{SS15}	120	–	–	ground 15
DAAB	121	I	Schmitt	data
WSAB	122	I	Schmitt	word strobe
EFAB	123	I	Schmitt	error flag
CLK34	124	O	2 mA	34 MHz output clock
TEST	125	I	Schmitt, PD25	test pin; must be ground
V_{SS16}	126	–	–	ground 16
DA0	127	O	S4	DRAM address bus; bit DA0
DA1	128	O	S4	DRAM address bus; bit DA1

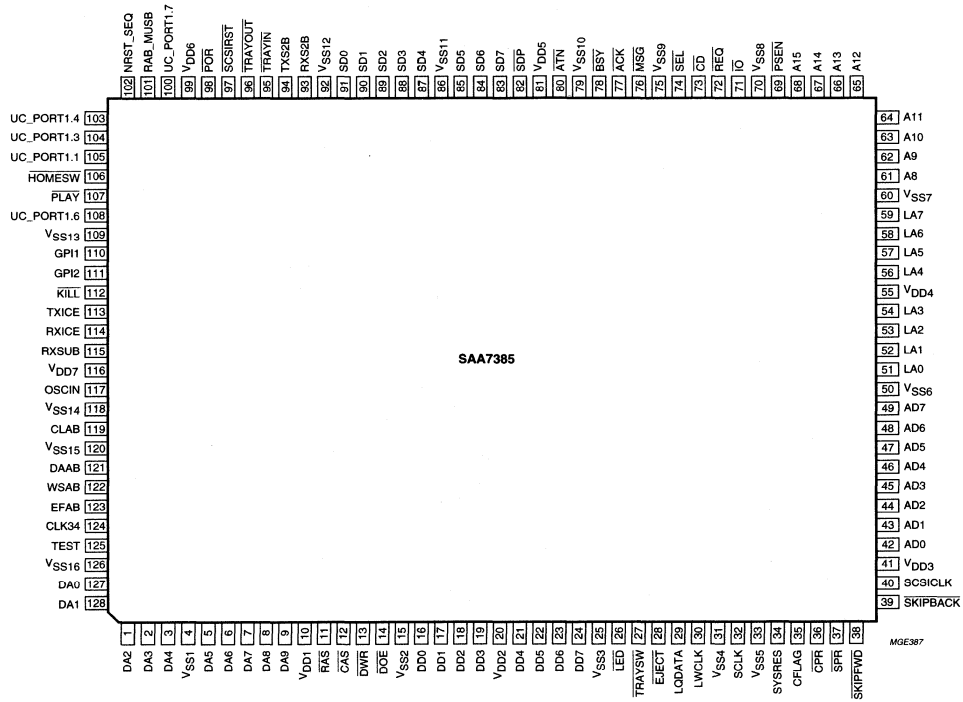


Fig.2 Pin configuration.

Error correction and host interface IC for CD-ROM (ELM)

SAA7388

CONTENTS

Error correction and host interface IC for CD-ROM (ELM)

SAA7388

1 FEATURES

- CD-ROM (Mode 1) and CD-I (Mode 2 - Form 1 and Form 2) formats supported
- Real-time error detection and correction in hardware
- Suitable for octal speed, n = 8.
- Maximum host transfer burst rate of 13.3 Mbyte/s
- Corrects two errors per symbol with erasure correction
- 36 kbit of on-chip error correction buffer RAM
- 12-byte command FIFO and 12-byte status FIFO
- Compatible with the Advanced Technology Attachment (ATA) register set and the Advanced Technology Attachment Program Interface (ATAPI) command set
- Operates with popular memories. (up to 128 kbyte SRAM; 1 to 16 Mbit DRAM, different speed grades, nibble or byte wide)
- Interface to Integrated Drive Electronics (IDE) bus without external bus drivers
- Q-to-W subcode buffering, de-interleaving and correction are supported
- Device can operate with audio RAMs. A RAM test allows bad segments to be identified.

2 GENERAL DESCRIPTION

The SAA7388 decoder is a block decoder buffer manager for high-speed CD-ROM applications that integrates real-time error correction and detection and host interface data transfer functions into a single chip.

The SAA7388 has an on-chip 36-kbit memory. This memory is used as a buffer memory for error and erasure corrections. The chip also has a buffer memory interface thus enabling the connection of SRAM up to 128 kbytes, or DRAM up to 16 Mbits. The on-chip memory is sufficient to buffer 1 sector of data. The external memory can buffer many more, depending on memory size.

The error corrector of the SAA7388 can perform 2-pass error correction in real-time. Buffer memory for this correction is integrated on-chip.

The SAA7388 has an host interface that is compatible with the SANYO LC89510 or OAK OTI-012 and also compatible with the ATA/IDE/ATAPI hard disc interface bus. (All ATAPI registers are present in hardware).

Supply of this Compact Disc IC does not convey an implied license under any patent right to use this IC in any Compact Disc application.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD1}	digital supply voltage 1	3.0	3.3	3.6	V
V_{DDD2}	digital supply voltage 2	4.5	5	5.5	V
I_{DDD}	supply current	–	60	–	mA
f_{clk}	clock frequency	15.2	48	50.4	MHz
T_{amb}	operating ambient temperature	0	–	+70	°C
T_{stg}	storage temperature	−55	–	+125	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7388GP	QFP80	plastic quad flat package; 80 leads; lead length 1.95 mm; body 14 × 20 × 2.8 mm	SOT318-2

5 BLOCK DIAGRAM

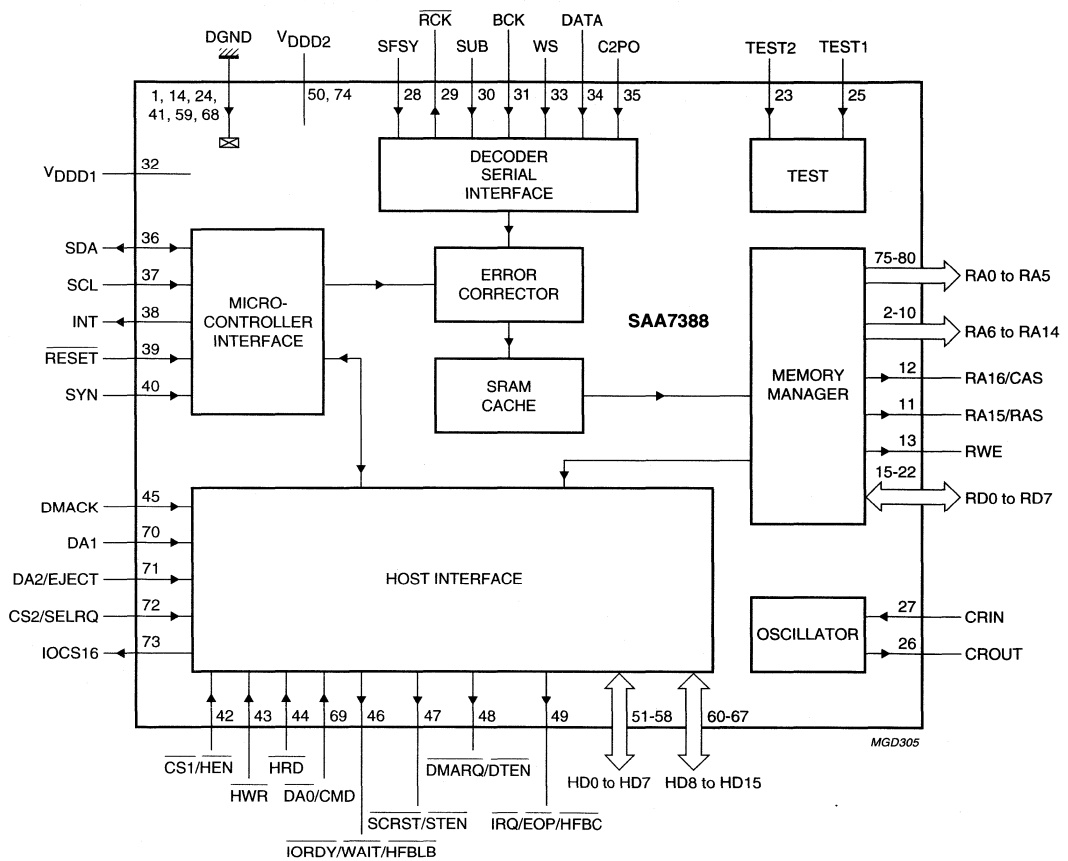


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	I/O	DESCRIPTION
DGND1	1	–	digital ground 1
RA6	2	O	buffer RAM address bus output line 6
RA7	3	O	buffer RAM address bus output line 7
RA8	4	O	buffer RAM address bus output line 8
RA9	5	O	buffer RAM address bus output line 9
RA10	6	O	buffer RAM address bus output line 10
RA11	7	O	buffer RAM address bus output line 11 (SRAM) only
RA12	8	O	buffer RAM address bus output line 12 (SRAM) only
RA13	9	O	buffer RAM address bus output line 13 (SRAM) only
RA14	10	O	buffer RAM address bus output line 14 (SRAM) only
RA15/RAS	11	O	buffer RAM address bus output line 15 (SRAM) or RAS (DRAM)
RA16/CAS	12	O	buffer RAM address bus output line 16 (SRAM) or CAS (DRAM)
RWE	13	O	buffer RAM write enable output
DGND2	14	–	digital ground 2
RD0	15	I/O	buffer RAM data bus bidirectional line 0
RD1	16	I/O	buffer RAM data bus bidirectional line 1
RD2	17	I/O	buffer RAM data bus bidirectional line 2
RD3	18	I/O	buffer RAM data bus bidirectional line 3
RD4	19	I/O	buffer RAM data bus bidirectional line 4
RD5	20	I/O	buffer RAM data bus bidirectional line 5
RD6	21	I/O	buffer RAM data bus bidirectional line 6
RD7	22	I/O	buffer RAM data bus bidirectional line 7
TEST2	23	I	test input 2
DGND3	24	–	digital ground 3
TEST1	25	I	test input 1
CROUT	26	O	clock oscillator output
CRIN	27	I	clock oscillator input
SFSY	28	I	serial subcode input frame sync input
$\overline{\text{RCK}}$	29	O	serial subcode clock output (active LOW)
SUB	30	I	serial input for Q-to-W subcode input
BCK	31	I	serial interface bit clock input
V_{DDD1}	32	–	digital supply voltage 1 (3.3 V)
WS	33	I	serial interface word clock input
DATA	34	I	serial data input
C2PO	35	I	serial interface flag input
SDA	36	I/O	sub-CPU serial data input/output
SCL	37	I	sub-CPU serial clock input
INT	38	O	sub-CPU open-collector interrupt output
$\overline{\text{RESET}}$	39	I	power-on reset input (active LOW)
SYN	40	I	sync signal input from sub-CPU

SYMBOL	PIN	I/O	DESCRIPTION
DGND4	41	–	digital ground 4
$\overline{CS1}/\overline{HEN}$	42	I	host interface enable input (active LOW)
$\overline{HWR}$	43	I	host interface write enable input (active LOW)
$\overline{HRD}$	44	I	host interface read enable input (active LOW)
DMACK	45	I	DMA acknowledge input
$\overline{IORDY}/\overline{WAIT}/\overline{HFBLB}$	46	O	host interface wait output (active LOW); 3-state control
$\overline{SCRST}/\overline{STEN}$	47	O	host interface status enable output ATAPI sub-CPU reset signal (active LOW)
$\overline{DMARQ}/\overline{DTEN}$	48	O	ATAPI DMA request host interface data enable output (active LOW); 3-state control
$\overline{IRQ}/\overline{EOP}/\overline{HFBC}$	49	O	host interface end of process flag output ATAPI host interrupt request (active LOW); 3-state control
V_{DDD2}	50	–	digital supply voltage 2 (5 V)
HD0	51	I/O	host interface data bus input/output line 0
HD1	52	I/O	host interface database input/output line 1
HD2	53	I/O	host interface database input/output line 2
HD3	54	I/O	host interface data bus input/output line 3
HD4	55	I/O	host interface data bus input/output line 4
HD5	56	I/O	host interface data bus input/output line 5
HD6	57	I/O	host interface data bus input/output line 6
HD7	58	I/O	host interface data bus input/output line 7
DGND5	59	–	digital ground 5
HD8	60	I/O	host interface data bus input/output line 8
HD9	61	I/O	host interface data bus input/output line 9
HD10	62	I/O	host interface data bus input/output line 10
HD11	63	I/O	host interface data bus input/output line 11
HD12	64	I/O	host interface data bus input/output line 12
HD13	65	I/O	host interface data bus input/output line 13
HD14	66	I/O	host interface data bus input/output line 14
HD15	67	I/O	host interface data bus input/output line 15
DGND6	68	–	digital ground 6
$\overline{DA0}$/CMD	69	I	host interface data input (active LOW)/command select input host interface address line 0
DA1	70	I	ATAPI address line input 1
DA2/EJECT	71	I	ATAPI address line input 2
CS2/SELRQ	72	I	ATAPI chip select input 2
IOCS16	73	O	ATAPI 16-bit data select output
V_{DDD2}	74	–	digital supply voltage 2 (5 V)
RA0	75	O	buffer RAM address bus output line 0
RA1	76	O	buffer RAM address bus output line 1
RA2	77	O	buffer RAM address bus output line 2

SYMBOL	PIN	I/O	DESCRIPTION
RA3	78	O	buffer RAM address bus output line 3
RA4	79	O	buffer RAM address bus output line 4
RA5	80	O	buffer RAM address bus output line 5

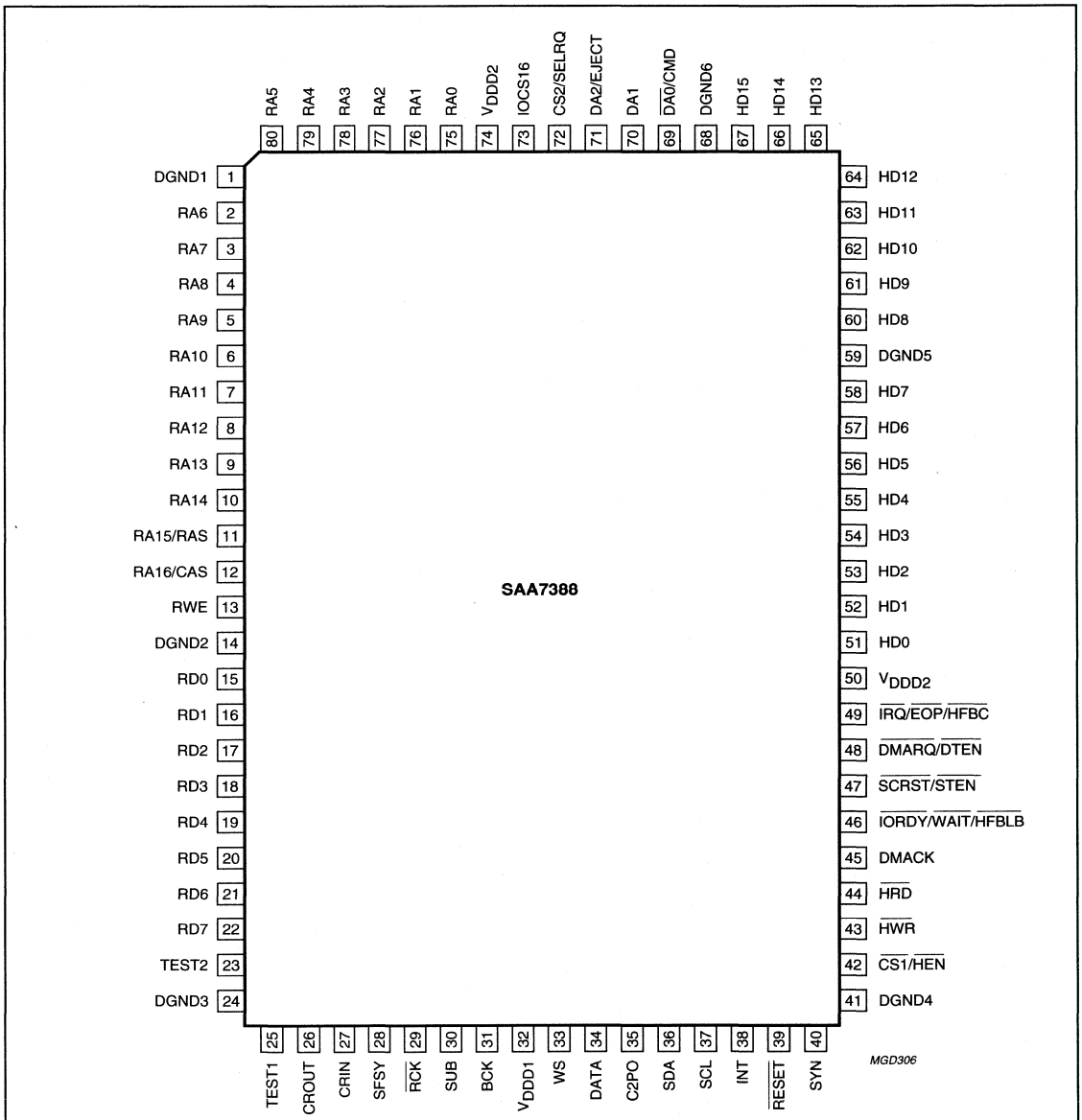


Fig.2 Pin configuration.

6.1 Pin functions

6.1.1 RA0 TO RA14

External memory address signals.

6.1.2 RA16/CAS

External memory RA16 signal if SRAM or, CAS signal if DRAM.

6.1.3 RA15/RAS

External memory RA15 signal if SRAM or, RAS signal if DRAM.

6.1.4 RWE

Write output enable signal for external buffer memory. This is LOW when the SAA7388 wants to write data into the external memory.

6.1.5 RD0 TO RD7

External buffer memory bidirectional data signals.

6.1.6 SFSY

Frame sync for the Q-to-W subcode, indicates when P-channel is available by a HIGH-to-LOW transition. Frame 0 is also indicated by no transition on this line.

6.1.7 $\overline{RCK}$

In response to SFSY going LOW data is clocked into the SAA7388 before each rising edge using this clock output.

6.1.8 SUB

Q-to-W subcode is input in response to $\overline{RCK}$ in 3-wire EIAJ mode or WS in "V4" mode compatible with the SAA7345.

6.1.9 BCK

Bit clock for the serial data input from the CD decoder.

6.1.10 WS

Word clock for the serial data input from the CD decoder.

6.1.11 DATA

Serial data input from the CD decoder. This may be either I^2S-bus or EIAJ 16-bit format.

6.1.12 C2PO

Error flag from the CD decoder. A HIGH indicates that a byte has not been corrected by the C2 error corrector and therefore is not valid. This is taken into account by the SAA7388 error corrector.

6.1.13 SDA

Sub-CPU bidirectional data signal. This signal forms part of the 3-wire serial interface between the SAA7388 and the sub-CPU.

6.1.14 SCL

Sub-CPU sync signal. This signal forms part of the 3-wire serial interface between the SAA7388 and the sub-CPU. This signal is used to synchronize data transfers between the sub-CPU and the SAA7388.

6.1.15 INT

Sub-CPU interrupt signal. This active LOW output signals to the sub-CPU that the SAA7388 has an interrupt request.

6.1.16 $\overline{RESET}$

Forcing this input LOW resets the SAA7388.

6.1.17 SYN

Sub-CPU clock signal. This signal forms part of the 3-wire serial interface between the SAA7388 and the sub-CPU. This signal is the sub-CPU driven bit clock used to synchronize the signals on the SDA line.

6.1.18 $\overline{CS1}/\overline{HEN}$

In the ATAPI mode this is the host chip select 1 address signal. In the Sanyo and Oak compatibility modes setting this input LOW enables the host interface.

6.1.19 $\overline{HWR}$

This active LOW signal is the host write request.

6.1.20 $\overline{HRD}$

This active LOW signal is the host read request.

6.1.21 DMACK

This signal is used in the ATAPI and Oak compatibility modes during DMA transfers. The host pulls this signal LOW in response to a $\overline{\text{DMARQ}}$ request to indicate that it is ready to transfer data.

If this signal is not being used then it must be pulled HIGH for SAA7388 to operate correctly.

6.1.22 $\overline{\text{IORDY}}/\overline{\text{WAIT}}/\overline{\text{HFBLB}}$

In the ATAPI mode this signal is negated to extend the host transfer cycle of any host register access. It is used in PIO transfers. When $\overline{\text{IORDY}}$ is not negated it is in a high-impedance state.

In the Sanyo compatibility mode the function of this signal depends on the SELRQ input. If SELRQ is HIGH then $\overline{\text{WAIT}}$ is set LOW to extend the host transfer cycle. If SELRQ is LOW then $\overline{\text{WAIT}}$ acts as the DRQ signal in a DMA transfer.

In the Oak compatibility mode this signal is the Host First Byte Latch signal. A rising edge on this signal is used to latch the first byte in a pseudo 16-bit DMA read. $\overline{\text{HFBLB}}$ can only be HIGH when pseudo 16-bit DMA transfer mode is selected.

6.1.23 $\overline{\text{SCRST}}/\overline{\text{STEN}}$

In the ATAPI or Oak compatibility mode this signal is pulled LOW to reset the sub-CPU in response to a reset command from the host.

In the Sanyo compatibility mode this signal is pulled LOW to signal to the host that status bytes are available for transfer.

6.1.24 $\overline{\text{DMARQ}}/\overline{\text{DTEN}}$

In the ATAPI or Oak compatibility mode this signal is asserted when the SAA7388 is ready to transfer data between the host and itself. In ATAPI single word and Oak DMA transfers this occurs at every word. In ATAPI multi-word DMA transfers this occurs at the start of the transfer.

In the Sanyo compatibility mode this signal is pulled LOW to signal to the host that data bytes are available for transfer.

6.1.25 $\overline{\text{IRQ}}/\overline{\text{EOP}}/\overline{\text{HFBC}}$

In the ATAPI mode this active HIGH signal indicates a host interrupt request. It is asserted when the sub-CPU writes to the ITRG register and is negated when the host reads the status register or writes to the command register.

In the Sanyo compatibility mode this signal is set LOW when the last data byte is transferred to or from the host.

In the Oak compatibility mode this is the Host First Byte Cycle output and is HIGH while the first byte in the pseudo 16-bit DMA transfer is accessed. It should be used to inhibit non-DMA transactions while the first byte is latched.

6.1.26 HD0 TO HD15

These are the bidirectional Host Data signals. In the Sanyo and Oak compatibility modes HD8 to HD15 are never used.

6.1.27 $\overline{\text{DA0}}$/CMD

In the ATAPI mode this is the host Data Address 0 signal. In the Sanyo and Oak compatibility modes this input selects between command or data transfers.

6.1.28 DA1

This is the ATAPI Data Address 1 signal.

6.1.29 DA2/ EJECT

In the ATAPI mode this is the Data Address 2 signal. In the Oak compatibility mode this is the door switch input pin. Its state is reflected in the TSTAT register.

6.1.30 CS2/SELRQ

In the ATAPI mode this is the Chip Select 2 signal. In the Oak and Sanyo compatibility mode this is the data transfer mode select input. It is used to select between PIO and DMA transfers.

6.1.31 IOCS16

This open-collector signal is used in the ATAPI mode to signal to the host that a 16-bit data port has been addressed. It is not activated during DMA transfers.

CONTENTS

1 FEATURES

- Supports real time error detection and correction in hardware. Error correction to n = 27, error detect to n = 30 and raw data transfer to n = 32.
- CD-R to CD-n greater than 8. Internal operation is faster, but firmware and physical (laser/media) factors limit the speed
- DVD-ROM supported in combination with the SAA7335
- Direct generic interface to external Small Computer Systems Interface (SCSI) controller devices
- Operates with up to 16 Mbytes DRAM
  - Hyper-page DRAM up to 33 Mbytes words/s burst
  - Fast-page DRAM at up to 17.5 Mbytes words/s burst
- Has fixed n = 1 or n = 2 rate (44.1 or 88.2 kHz) I^2S-bus multimedia output for simple audio/video output; features for CAV/quasi-CLV support
  - Supports Philips multimedia audio CODEC
  - Provides 'SHOARMA' Red Book audio buffer
- IEC 958 (SPDIF, AES/EBU and DOBM) output with Q-W subcode and programmable category code, output at n = 1 rate
- Device registers are memory mapped for faster direct access to the chip
- Provides direct access from sub-CPU to buffer RAM to support scratchpad accesses. This eliminates the need for extra RAM chips in the system
- Automatic sequencing of ATAPI packet command protocol, including command termination
- Automated data transfers to and from the host using PIO, DMA and ultra DMA.

2 GENERAL DESCRIPTION

The SAA7391 is a block decoder/encoder and buffer manager for high-speed CD-ROM/CD-R functions, that integrates real time error correction and detection and bidirectional ATAPI transfer functions into a single chip.

2.1 Memory mapped control registers

The SAA7391 device has a large number of memory mapped registers. These are arranged so that high-level languages see the registers as external byte or 16-bit integer quantities. The block addressing of the SAA7391 facilitates the use of pairs of 16-bit quantities to represent addresses.

The reading and writing of 16-bit registers within the device can be performed by two separate 8-bit reads, where the second byte data is latched at the same time as the first byte is read.

2.2 Error correction features

The SAA7391 has an on-chip 36 kbits memory that is used as a buffer memory for error and erasure correction processing. This buffer memory reduces the number of external RAM accesses that are needed for error correction and thus allows for an increased rate of data throughput.

The error corrector is switchable between two-pass, single-pass [both with Error Detection/Correction (EDC)] and EDC only modes to further improve throughput. The presence of the full error corrector removes the need for firmware based control of the error corrector's operation.

2.3 Host interface features

The SAA7391 has an ATAPI host interface that may be directly connected to the ATAPI bus thereby reducing the need for external support devices. It supports PIO Mode 4 transfer and Mode 0 ultra DMA. This interface can also be configured as a generic DMA interface for use with external host interface devices (e.g. SCSI controller). The DMA interface has the following features:

- ATAPI command packets are automatically loaded into the command FIFO
- Data transfer to the host is automatically sequenced to reduce inter-block latencies and improve host CPU utilisation
- Host data transfer rate is independent of error corrector operation and the data input path
- The host interface features automatic determination of block length for Mode 2, Form 1 and Form 2 sectors. The block length transferred is programmable.
- The host interface can transfer up to 3 sub-blocks per sector, with each sub-block being transferred dependent on the Form bit. Automatic reload of sub-block pointers and unconditional transfer are supported.

2.4 Buffer memory organisation

Memory is mapped as a 16-bit block number and 12-bit offset into that block. The block oriented memory structure permits the use of 16-bit pointers in software thereby minimising the overhead of accessing memory.
The address can be found from the following equation:
address = block number × 2560 + offset.

The microcontroller sees the SAA7391 as a memory mapped peripheral, with control and status registers appearing in the upper address space.

The lowest 52 kbytes (48 kbytes + 4 kbytes) of the 8051 microcontroller external address space is mapped as a window into the memory on a user-specified 1 kbyte boundary within the buffer RAM. This can be used as a scratchpad memory.

The next 4 kbytes is separately mapped as a window into the memory on a user-specified 1 kbyte boundary within the RAM.

The next 7.5 kbytes of the external data space consists of three independently addressed memory segments for accessing block data, subcode information and block headers.

The registers of the SAA7391 are mapped into the top 256 bytes of external data space.

2.5 Subcode handling features

The writing of data into the buffer RAM is aligned to the absolute time sync marker with the following features:

- Subcodes are written into memory together with their associated sector data.This eases the provision of specialist features, for example CD + G or Karaoke CD applications.
- All channels of subcode are de-interleaved
- The Q channel is also Cyclic Redundancy Checked (CRC) for increased reliability
- When operating in 3-wire subcode mode, it is possible to control or read the P bit in the P-W subcode stream.

2.6 Multimedia output audio control features

The I²S-bus input may be processed before feeding to the multimedia audio output in several simple ways:

- As audio is transferred via the buffer memory, it is not necessary to have the CD-DSP I²S-bus input at exactly the audio n = 1 or video n = 2 rate. Any faster speed will work because the buffer RAM is used as a FIFO.
- Both channels may be independently controlled. The left channel output may be sourced from zero (digital silence), left or right input; this also applies for the right channel output. This permits basic audio switching and channel swapping.
- IEC 958 (SPDIF, AES/EBU and DOBM) output with Q-W subcode and programmable category code, can be output from the same CD-DSP I²S-bus data source.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{DDD(core)}$	digital core supply voltage	3.0	3.3	3.6	V
$V_{DDD(pad)}$	digital peripheral supply voltage	$V_{DDD(core)}$	5.0 or 3.3	5.0	V
I_{DDD}	supply current	tbf	60	tbf	mA
f_{xtal}	crystal frequency	8	8.4672, 11.289, 16.9344 or 33.8688	35	MHz
T_{amb}	operating ambient temperature	0	–	70	°C
T_{stg}	storage temperature	–55	–	+125	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7391H	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1

5 BLOCK DIAGRAM

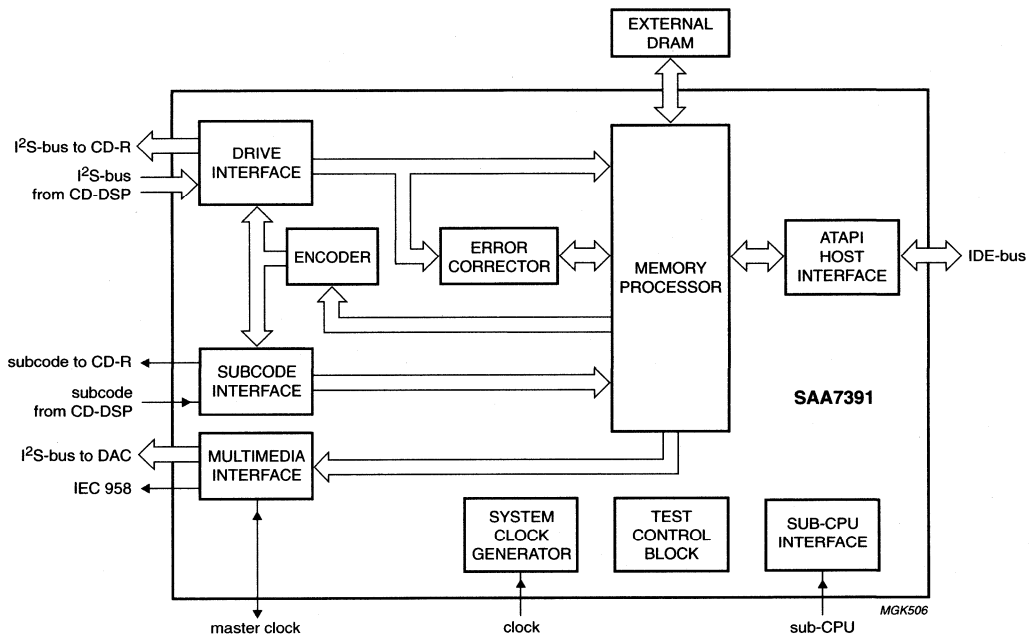


Fig.1 The SAA7391 internal block diagram.

6 PINNING

SYMBOL	PIN	TYPE	DRIVE/ THRESHOLD	GROUPING	DESCRIPTION
n.c.	1	–	–	–	not connected
n.c.	2	–	–	–	not connected
XDA0	3	O	M	RAM	output address lines
XDA1	4	O	M		
XDA2	5	O	M		
$V_{DDD(pad6)}$	6	–	–	–	digital peripheral supply voltage 6
DGND1	7	–	–	–	digital ground 1
XDA3	8	O	M	RAM	output address lines
XDA4	9	O	M		
XDA5	10	O	M		
XDA6	11	O	M		
XDA7	12	O	M		
XDA8	13	O	M		
XDA9	14	O	M		
XDA10	15	O	M		
XDA11	16	O	M		
DGND2	17	–	–	–	digital ground 2
$\overline{XRAS}$	18	O	H	RAM	row address strobe output (active LOW)
$\overline{XCAS}$	19	O	H		column address strobe output (active LOW)
$\overline{XWR}$	20	O	H		write enable output (active LOW)
XDD0	21	I/O	M/T	RAM	data bus input/output
XDD1	22	I/O	M/T		
$V_{DDD(core1)}$	23	–	–	–	digital core supply voltage 1
DGND3	24	–	–	–	digital ground 3
XDD2	25	I/O	M/T	RAM	data bus input/output
XDD3	26	I/O	M/T		
XDD4	27	I/O	M/T		
XDD5	28	I/O	M/T		
XDD6	29	I/O	M/T		
XDD7	30	I/O	M/T		
$V_{DDD(pad7)}$	31	–	–	–	digital peripheral supply voltage 7
DGND4	32	–	–	–	digital ground 4
SCKI1	33	I	C	I^2S-bus I/O	I^2S-bus bit clock input
WSI1	34	I	C		I^2S-bus word select strobe input

SYMBOL	PIN	TYPE	DRIVE/ THRESHOLD	GROUPING	DESCRIPTION
n.c.	35 to 38	–	–	–	not connected
SDI1	39	I	C	I^2S-bus I/O	data input from CD engine
SDO1	40	O	M		data output to CD-R writer
SFSY	41	I/O	L/C	subcode I/O	3-wire subcode sync input/output
RCK	42	I/O	L/C		3-wire subcode clock input/output
SUBI	43	I	C		Q and R-W subcode input
SUBO	44	O	L		subcode output from encoder to writer
CFLG	45	I	C	I^2S-bus input	CD error corrector flags and absolute time sync
C2P0	46	I	C		CD C2 error correction flag input for ERCO
DGND5	47	–	–	–	digital ground 5
IECO	48	O	M	multimedia	IEC 958 output
MCK	49	I/O	M/C	multimedia output	$256f_s$ or $384f_s$ clock for multimedia master clock/IEC 958 clock or divided system clock for CD-DSP
SCK2	50	I/O	L/C	multimedia	I^2S-bus bit clock input/output
WS2	51	I/O	L/C		I^2S-bus word select strobe input/output
SDO2	52	O	M		I^2S-bus data output to DAC/video decoder
GND	53	–	–	–	ground
CROUT	54	O	crystal pad	crystal oscillator	crystal oscillator output
CRIN	55	I	crystal pad		crystal oscillator/clock input
V_{DDA}	56	–	–	–	analog supply voltage
I_{ref}	57	analog	current input	clock generator	VCO reference current
$\overline{POR}$	58	I	Schmitt trigger	system	power-on reset (active LOW)
TEST1	59	I	C	test	mode control input test pins
TEST2	60	I	C		
$\overline{RESET}$	61	I	Schmitt trigger	host	ATAPI bus reset input from host (active LOW)
DD7	62	I/O	AL/T	host	data bus input/output
DD8	63	I/O	AL/T		
DD6	64	I/O	AL/T		
$V_{DDD(pad1)}$	65	–	–	–	digital peripheral supply voltage 1
DGND6	66	–	–	–	digital ground 6
DD9	67	I/O	AL/T	host	data bus pin order of ATAPI interface matches the pinning of the 40-way IDE connector (slew rate limiting by control of drive capability into capacitive load of ATA bus)
DD5	68	I/O	AL/T		
DD10	69	I/O	AL/T		
DD4	70	I/O	AL/T		

SYMBOL	PIN	TYPE	DRIVE/ THRESHOLD	GROUPING	DESCRIPTION
n.c.	71 to 74	–	–	–	not connected
DD11	75	I/O	AL/T	host	data bus; pin order of ATAPI interface matches the pinning of the 40-way IDE connector (slew rate limiting by control of drive capability into capacitive load of ATA bus)
DD3	76	I/O	AL/T		
DD12	77	I/O	AL/T		
DD2	78	I/O	AL/T		
DD13	79	I/O	AL/T		
DD1	80	I/O	AL/T		
DD14	81	I/O	AL/T		
DD0	82	I/O	AL/T		
DD15	83	I/O	AL/T		
DMARQ/ $\overline{\text{DMACK}}$	84	O	AL	host	DMA request/SCSI DMA acknowledge output (active LOW)
DGND7	85	–	–	–	digital ground 7
$V_{DDD(pad2)}$	86	–	–	–	digital peripheral supply voltage 2
$\overline{\text{DIOW}}$	87	I	L/T	host	write cycle write enable/control register write input (active LOW)
$\overline{\text{DIOR}}$	88	I	L/T	host	read cycle read enable/control register read input (active LOW)
$\overline{\text{IORDY}}$	89	O	AH	host	device is ready to transfer data output (active LOW)
$\overline{\text{DMACK}}$/ DMARQ	90	I	T	host	DMA acknowledge (active LOW)/SCSI DMA request input
INTRQ	91		A	host	host interrupt request (NB 3-state output)
DGND8	92	–	–	–	digital ground 8
$V_{DDD(pad3)}$	93	–	–	–	digital peripheral supply voltage 3
$\overline{\text{IOCS16}}$	94	O	AH	host	I/O port is 16-bit output (active LOW)
DA1/$\overline{\text{DBWR}}$	95	I/O	L/T	host	address wire 1/DMA from generic interface is output from the SAA7391 (active LOW)
$\overline{\text{PDIAG}}$	96	I/O	AL/T	host	ATAPI passed diagnostics input/output (active LOW)
DA0	97	I/O	L/T	host	address wire 0 input/output
DA2/$\overline{\text{DBRD}}$	98	I/O	L/T	host	address wire 2/DMA from generic interface is input to the SAA7391 (active LOW)
$\overline{\text{CS0}}$/ $\overline{\text{SCSICS}}$	99	I/O	L/T	host	chip select 1FX/generic interface chip select (active LOW)
$\overline{\text{CS1}}$	100	I/O	L/T	host	chip select 3FX input/output (active LOW)
$\overline{\text{DASP}}$	101	I/O	AH/T	host	device active slave present input/output (active LOW)
INT2	102	O	L	sub-CPU	sub-CPU interrupt output from the SAA7391 drive block and UART

SYMBOL	PIN	TYPE	DRIVE/ THRESHOLD	GROUPING	DESCRIPTION
DGND9	103	–	–	–	digital ground 9
$V_{DDD(pad4)}$	104	–	–	–	digital peripheral supply voltage 4
COMACK	105	I	C	UART	command acknowledge/transmit flow control input
COMCLK	106	O	L	UART	serial data clock for synchronous mode output
n.c.	107 to 110	–	–	–	not connected
COMOUT	111	O	L	UART	transmit data output
COMIN	112	I	C	UART	receive data input
COMSYNC	113	I	C	UART	basic engine synchronization input
SYSSYNC	114	I	C	UART	basic engine synchronization input
SCCLK	115	O	M	sub-CPU	sub-CPU clock output
$\overline{RD}$	116	I	T	sub-CPU	sub-CPU read enable (active LOW)
$\overline{WR}$/R/$\overline{W}$	117	I	T	sub-CPU	sub-CPU write enable/and read/write control input (active LOW)
$\overline{INT}$	118	O	L	sub-CPU	sub-CPU interrupt request output from host interface (active LOW)
SRST	119	O	L	sub-CPU	sub-CPU reset output
SCA0/SCD0	120	I/O	L/T	sub-CPU	multiplexed address/data lines
SCA1/SCD1	121	I/O	L/T		
DGND10	122	–	–	–	digital ground 10
$V_{DDD(pad5)}$	123	–	–	–	digital peripheral supply voltage 6
SCA2/SCD2	124	I/O	L/T	sub-CPU	multiplexed address/data lines
SCA3/SCD3	125	I/O	L/T		
SCA4/SCD4	126	I/O	L/T		
SCA5/SCD5	127	I/O	L/T		
SCA6/SCD6	128	I/O	L/T		
SCA7/SCD7	129	I/O	L/T		
DGND11	130	–	–	–	digital ground 11
$V_{DDD(core2)}$	131	–	–	–	digital core supply voltage 2
ALE	132	I	T	sub-CPU	demultiplex enable input for lower address lines
$\overline{PSEN}$	133	I	T	sub-CPU	program store enable (active LOW)
SCA15	134	I	T	sub-CPU	upper address lines input
SCA14	135	I	T		
SCA13	136	I	T		
SCA12	137	I	T		
DGND12	138	–	–	–	digital ground 12

SYMBOL	PIN	TYPE	DRIVE/ THRESHOLD	GROUPING	DESCRIPTION
SCA11	139	I	T	sub-CPU	upper address lines input
SCA10	140	I	T		
SCA9	141	I	T		
SCA8	142	I	T		
n.c.	143	–	–	–	not connected
n.c.	144	–	–	–	not connected

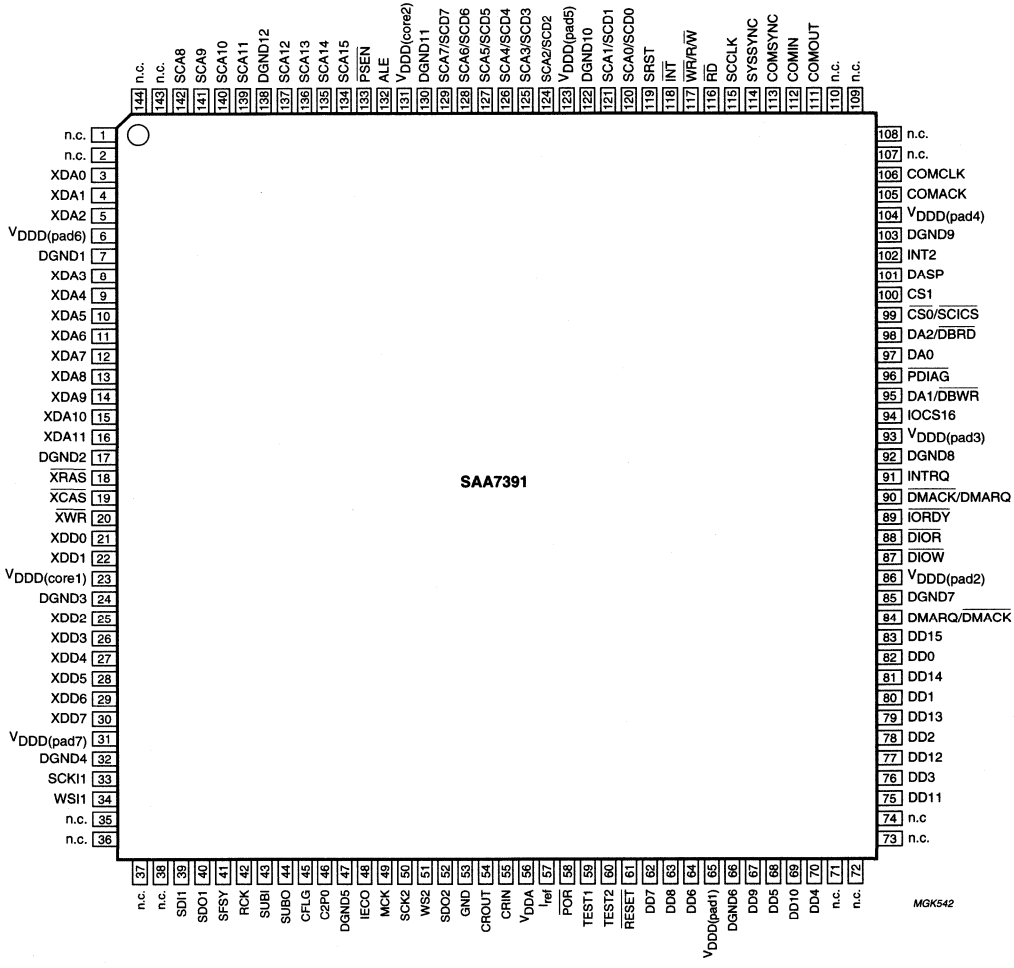


Fig.2 Pin configuration.

6.1 Detailed description of pin functions

Table 1 Q and R-W input/output subcode connections (4 pins)

SYMBOL	DESCRIPTION	COMMENT
SFSY	3-wire subcode sync	input subcode frame sync for receiving 3-wire subcode; output subcode frame sync for transmitting 3-wire subcode
RCK	3-wire subcode clock	output bit clock for receiving 3-wire subcode; input bit clock for transmitting 3-wire subcode
SUBI	Q and R-W subcode input	configurable for 3-wire or Philips V4 subcode mode; can use either RCK or WSI1 as clock references with appropriate dividers
SUBO	output subcode from encode	configurable for Philips SRI (Subcode Recordable Interface) 3-wire or Philips V4 subcode mode; can use either RCK, WSI1 or WS2 as clock references

Table 2 I^2S-bus multimedia audio output (5 pins)

SYMBOL	DESCRIPTION	COMMENT
MCK	$256f_s$ or $384f_s$ clock for multimedia master clock/IEC 958 clock or divided system clock for CD-DSP	Clock reference input pin when interface is in a master mode; a programmable divider is provided. This pin is also configurable as a programmable clock output intended as a clock reference for a CD-DSP. Should be pulled up if not in use.
SCK2	I^2S-bus bit clock	This is used for master and slave I^2S-bus application as both modes are needed. For instance, the Philips multimedia CODEC is an I^2S-bus slave, hence this must be a master interface. When driving some DACs, this interface can be a slave.
WS2	I^2S-bus left/right strobe	word select strobe either master or slave
SDO2	I^2S-bus data to DAC/video decoder	I^2S-bus multimedia data
IECO	IEC 958 output	the IEC 958 output combines multimedia data and Q-W subcode

Table 3 I^2S-bus connections to CD engine (6 pins)

SYMBOL	DESCRIPTION	COMMENT
SCKI1	I^2S-bus bit clock	this is a separate clock to the multimedia bit clock as this rate is derived from the disc linear velocity
WSI1	I^2S-bus left/right strobe	
SDI1	I^2S-bus data from CD-DSP	
SDO1	I^2S-bus data to CD-writer	
C2P0	CD C2 error corrector flag from ERCO	these flags are used to indicate errors from second layer correction to the ERCO
CFLG	CD error corrector flags and absolute time sync	The absolute time sync is used in the CD input process for playing 'Red Book' discs; the error corrector status is also read in from this signal, to provide an indication of C1 and C2 performance for CD-RW applications.

Table 4 ATAPI target mode interface

ATAPI NAME	ATAPI MEANING
$\overline{\text{RESET}}$	ATAPI reset signal: the SAA7391 will not recognize a signal assertion shorter than 20 ns as a valid reset signal.
DD0 to DD7	ATAPI D0 to D7
DD8 to DD15	ATAPI D8 to D15: these data bits are only used in accesses to the 16-bit data port
DMARQ	DMA request: this signal, used for DMA data transfers between host and device, is asserted by the SAA7391 when it is ready to transfer data to or from the host. The direction of data transfer is controlled by $\overline{\text{DIOR}}$ and $\overline{\text{DIOW}}$.
$\overline{\text{DMACK}}$	DMA acknowledge: this signal is used by the host in response to DMARQ to initiate DMA transfers. This signal may be temporarily negated by the host to suspend the DMA transfer in process.
$\overline{\text{IOCS16}}$	ATAPI I/O port is a 16-bit open-drain output: during PIO transfer Modes 0, 1 or 2, $\overline{\text{IOCS16}}$ indicates to the host system that the 16-bit data port has been addressed and that the device is prepared to send or receive a 16-bit data word.
$\overline{\text{IORDY}}$	ATAPI I/O ready open-drain output: this signal is negated to extend the host transfer cycle of any host register access (read or write) when the SAA7391 is not ready to respond to a data transfer request. This signal is only enabled during $\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ cycles to the SAA7391. When $\overline{\text{IORDY}}$ is not active, it is in the high-impedance (undriven) state.
DA0 to DA2	address bus (device address)
$\overline{\text{DIOW}}$	ATAPI write strobe: the rising edge of $\overline{\text{DIOW}}$ latches data from the signals, DD0 to DD7 or DD0 to DD15 into a register or the data port of the SAA7391. The SAA7391 will not act on the data until it is latched.
$\overline{\text{DIOR}}$	ATAPI read strobe: the falling edge of $\overline{\text{DIOR}}$ enables data from a register or data port of the SAA7391 onto the signals, DD0 to DD7 or DD0 to DD15. The rising edge of $\overline{\text{DIOR}}$ latches data at the host and the host will not act on the data until it is latched.
$\overline{\text{CS0}}$	ATAPI chip select 0 input: this is the chip select signal from the host used to select the ATA command block registers. This signal is also known as $\overline{\text{CS1FX}}$.
$\overline{\text{CS1}}$	ATAPI chip select 1 input: this is the chip select signal from the host used to select the ATA control block registers. This signal is also known as $\overline{\text{CS3FX}}$.
INTRQ	ATAPI interrupt output: this signal is used to interrupt the host system. INTRQ is asserted only when the device has a pending interrupt, the device is selected, and the host has cleared the 'nien' bit in the device control register. If the 'nien' bit is equal to 1, or the device is not selected, this output is in a high-impedance state, regardless of the presence or absence of a pending interrupt.
$\overline{\text{PDIAG}}$	ATAPI passed diagnostics: this signal shall be asserted by device 1 to indicate to device 0 that it has completed diagnostics.
$\overline{\text{DASP}}$	ATAPI DASP (device active, device 1 present): this is a time-multiplexed signal which indicates that a device is active, or that device 1 is present. This signal is an open-drain output.

Table 5 Generic host controller interface

ATAPI NAME	GENERIC INTERFACE NAME	GENERIC HOST CONTROLLER INTERFACE MEANING
$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	controller reset output
DD0 to DD7	D0 to D7	controller DMA path/controller data and control bus (optional)
DD8 to DD15	D8 to D15	controller upper DMA path (optional)
DMARQ	$\overline{\text{DMACK}}$	DMA acknowledge to controller
$\overline{\text{DMACK}}$	DMARQ	DMA request from controller
DA1	$\overline{\text{DBWR}}$	DMA bus write to controller
DA2	$\overline{\text{DBRD}}$	DMA bus read from controller
$\overline{\text{CS0}}$	$\overline{\text{SCSICS}}$	controller chip select output for sub-CPU read/write cycles

Table 6 Miscellaneous pins

SYMBOL	DESCRIPTION	COMMENT
CRIN	crystal oscillator/clock input	–
CROUT	crystal oscillator output	–
I_{ref}	VCO reference current	clock PLL multiplier
$\overline{\text{POR}}$	power-on reset pin	–
TEST1 and TEST2	mode control test pins	–

Table 7 Sub-CPU interface pins

SYMBOL	DESCRIPTION	COMMENT
SRST	sub-CPU reset	active HIGH reset if XDD7 is pulled LOW during power-on reset; active LOW reset if XDD7 is pulled HIGH during power-on reset
$\overline{\text{INT}}$	sub-CPU interrupt request output from host interface	open-drain sub-processor interrupt from host interface
INT2	sub-CPU interrupt output from the SAA7391 drive block and UART	open-drain sub-processor interrupt from drive and UART
SCCLK	sub-CPU clock out	–
$\overline{\text{RD}}$	sub-CPU read enable	sub-CPU read enable strobe; if grounded permanently, the $\overline{\text{WR}}$ signal will act as read/write control input
$\overline{\text{WR}}$/R/$\overline{\text{W}}$	sub-CPU write enable/ read/write control	write enable; alternative usage is read/$\overline{\text{write}}$ if $\overline{\text{RD}}$ is held LOW at all times; $\overline{\text{WR}}$ has priority over $\overline{\text{RD}}$ at all times
ALE	demultiplex enable input for lower address lines	while HIGH, the lower address bits are latched from SCD0 to SCD7; should be used with a Schmitt trigger input to avoid false latching due to ground bounce on the 8051 microcontroller

SYMBOL	DESCRIPTION	COMMENT
$\overline{PSEN}$	program store enable	if this pin is LOW then the 8051 microcontroller is accessing external program store; this pin is used as an active HIGH chip enable
SCD0 to SCD7/ SCA0 to SCA7	sub-CPU data bus multiplexed/low address bus	–
SCA8 to SCA15	sub-CPU address high bits	–

Table 8 RAM interface pins

SYMBOL	DESCRIPTION	COMMENT
XDA0 to XDA11	RAM address bits, multiplexed for DRAM	up to 16 Mbytes DRAM only supported
$\overline{XRAS}$	DRAM row address strobe	
$\overline{XCAS}$	DRAM column address strobe	
$\overline{XWR}$	RAM write enable	
XDD0 to XDD7	RAM data bus	

Table 9 Basic engine interface

SYMBOL	DESCRIPTION	COMMENT
SYSSYNC	basic engine synchronization input	generate interrupts on rising and/or falling edges
COMSYNC	basic engine synchronization input	generate interrupts on rising and/or falling edges
COMIN	receive data	–
COMOUT	transmit data	–
COMCLK	serial data clock for synchronous mode	–
COMACK	command acknowledge/transmit flow control	must be HIGH for synchronous mode to transmit next data byte

Digital satellite radio broadcasting tuner decoder (SAT-2)

SAA7500

GENERAL DESCRIPTION

The SAA7500 performs a decoder function for digital satellite sound broadcasting tuners. It is designed to decode one of 16 stereo channels broadcasting audio signals in accordance with the German standard - **Technische Richtlinie ARD/ZDF Nr. 3R1**.

Features

- Clock recovery
- Differential decoding
- Main frame synchronization
- Swapping half-frames in case of inversion
- Unscrambling
- Demultiplexing
- Subframe synchronization
- Error correction and concealment
- Scale factor decoding with error correction
- Shift into the original values using the scale factors
- Mute in case of synchronization loss

QUICK REFERENCE DATA

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Supply voltage	V_{DD}	4.5	5.5	V
Power dissipation	P_{tot}		500	mW
Clock frequency	T_{20N}	20.48		MHz

PACKAGE OUTLINE

68-lead plastic leaded chip carrier (PLCC); 'pocket' version (SOT188AA); SOT188-2; 1996 September 05.

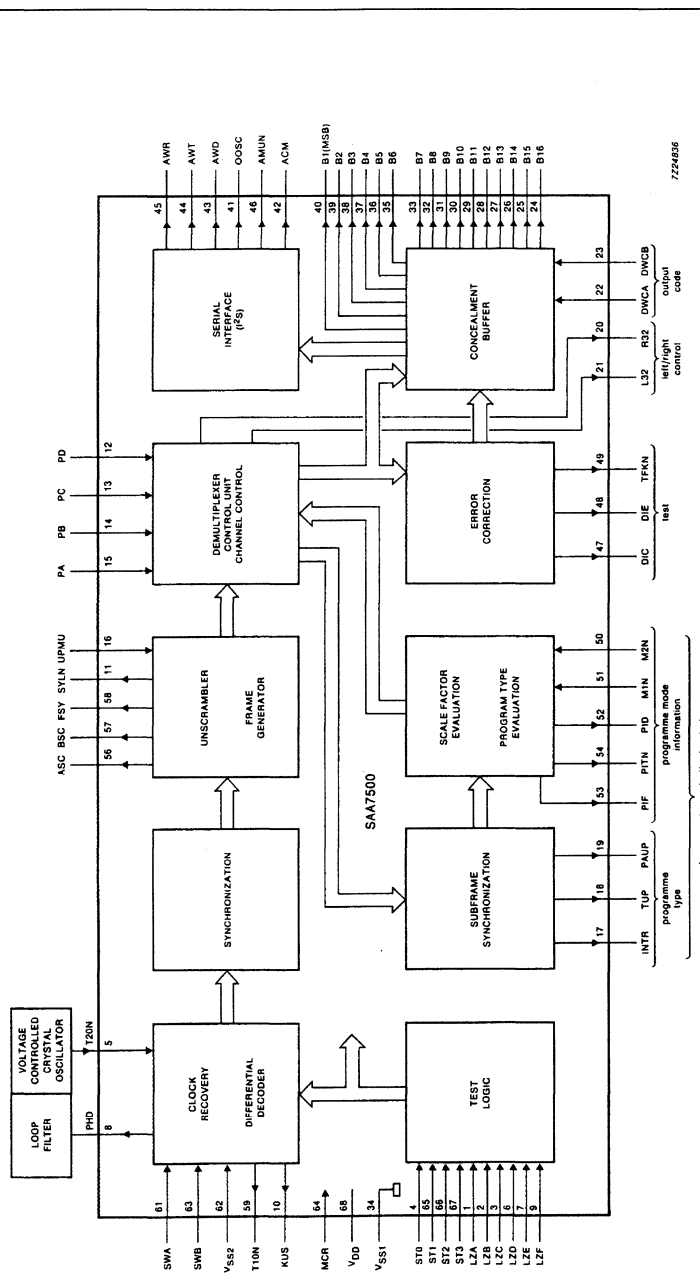


Fig.1 Block diagram.

PINNING

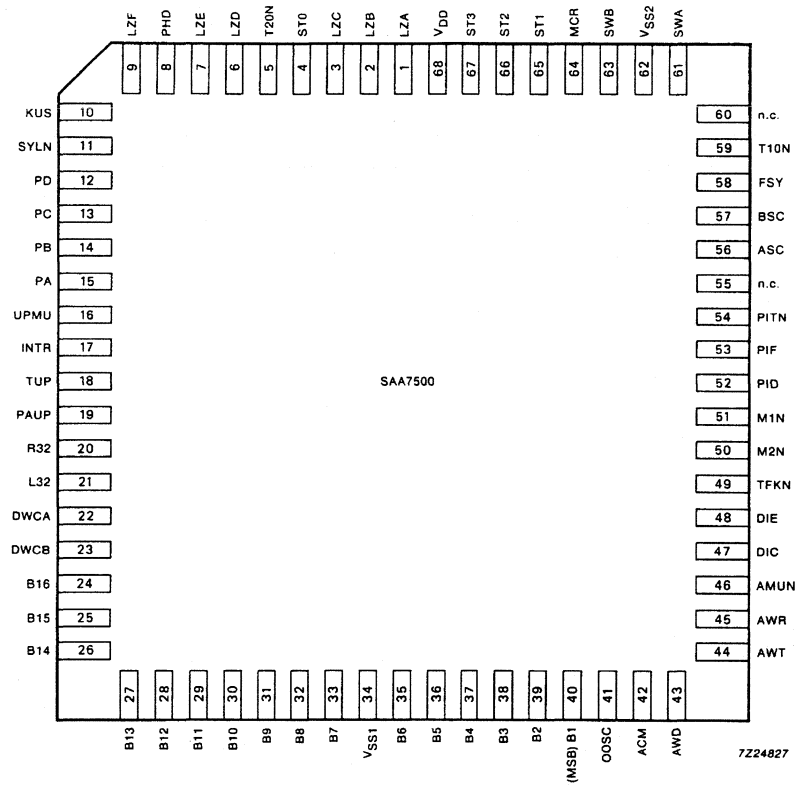


Fig.2 Pinning diagram; for pin functions see next page.

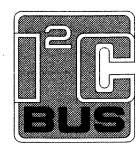
Pin functions

(1) = CMOS level input. (2) = TTL level input. (3) = CMOS level input with pull down resistor.

PIN NO.	MNEMONIC		DESCRIPTION
1	LZA	I(3)	phase adjustment for the internal clock.
2	LZB	I(3)	phase adjustment for the internal clock.
3	LZC	I(3)	phase adjustment for the internal clock.
4	STO	I(3)	control input for testing.
5	T20N	I(1)	20.48 MHz clock input from voltage controlled oscillator (VCX).
6	LZD	I(3)	control input for testing.
7	LZE	I(3)	control input for testing.
8	PHD	O	phase control signal for VCX.
9	LZF	I(3)	control input for testing.
10	KUS	O	test output (A'B' swap).
11	SYLN	O	synchronization indication flag.
12	PD	I(2)	programme number input selector (MSB).
13	PC	I(2)	programme number input selector.
14	PB	I(2)	programme number input selector.
15	PA	I(2)	programme number input selector (LSB).
16	UPMU	I(2)	mute input (controlled by microcomputer).
17	INTR	O	interrupt flag for microcomputer.
18	TUP	O	programme type interface (clock).
19	PAUP	O	programme type interface (data).
20	R32	O	multiplex control signal for right channel.
21	L32	O	multiplex control signal for left channel.
22	DWCA	I(3)	DA-converter mode select input.
23	DWCB	I(3)	DA-converter mode select input.
24-33	B16-7	O	audio data for parallel interface, bits 16 (LSB) to 7.
34	V_{SS1}	I	ground (supply).
35-40	B6-1	O	audio data for parallel interface, bits 6 to 1 (MSB).
41	OOSC	O	4.096 MHz clock output.
42	ACM	O	concealment flag (for SAA7220P/C).
43	AWD	O	audio data (for SAA7220P/C).
44	AWT	O	bit clock (for SAA7220P/C).
45	AWR	O	word select signal (for SAA7220P/C).
46	AMUN	O	mute signal (for SAA7220P/C).
47	DIC	O	data output for testing.
48	DIE	O	data output for testing.

PIN NO.	MNEMONIC		DESCRIPTION
49	TFKN	O	burst clock for test data.
50	M2N	I(2)	channel mode select input.
51	M1N	I(2)	channel mode select input.
52	PID	O	programme information (PI) interface output (data).
53	PIF	O	programme information (PI) interface output (window signal).
54	PITN	O	programme information (PI) interface output (clock).
55	n.c.		not connected.
56	ASC	O	data output for 10.24 Mbit/s interface.
57	BSC	O	data output for 10.24 Mbit/s interface.
58	FSY	O	window signal for 10.24 Mbit/s interface.
59	T10N	O	10.24 MHz clock output.
60	n.c.		not connected.
61	SWA	I(2)	10.24 Mbit/s data input.
62	V_{SS2}	I	ground (screen).
63	SWB	I(2)	10.24 Mbit/s data input.
64	MCR	I(1)	master reset.
65	ST1	I(3)	control input for testing.
66	ST2	I(3)	control input for testing.
67	ST3	I(3)	control input for testing and mode select for 10.24 Mbit/s interface.
68	V_{DD}	I	power supply.

CONTENTS



Car radio Digital Signal Processor (CDSP) SAA7707H

1 FEATURES

1.1 Hardware

- Bitstream 3rd-order Sigma-Delta Analog-to-Digital Converters (ADCs) with anti-aliasing broadband input filters
- Digital-to-Analog Converters (DACs)with four times oversampling and noise shaping
- Digital stereo decoder
- Improved digital Interference Absorption Circuit (IAC)
- RDS processing with optional 16-bit buffer via separate channel (two-tuner radio possible)
- Auxiliary analog CD input (CD-walkman, speech, economic CD-changer, etc.)
- Two separate full I²S-bus CD and DCC high performance interfaces
- Expandable with additional Digital Signal Processors (DSPs) for sophisticated features through an I²S-bus gateway
- Audio output short-circuit protected
- I²C-bus controlled
- Analog tape input
- Operating ambient temperature from −40 to +85 °C.

1.2 Software

- Improved FM weak signal processing
- Integrated 19 kHz MPX filter and de-emphasis
- Electronic adjustments: FM/AM level, FM channel separation and Dolby level
- Baseband audio processing (treble, bass, balance, fader and volume)
- Dynamic loudness or bass boost
- Stereo one-band parametric equalizer
- Audio level meter for an automatic leveller (in combination with microcontroller)
- Tape equalization (DCC analog playback)
- Music Search detection for Tape (MSS)
- Pause detection for RDS updates
- Dolby-B tape noise reduction
- Adjustable dynamics compressor
- CD and DCC de-emphasis processing
- Signal level, noise and multi-path detection for RDS (I²C-bus command)
- Improved AM reception.

2 APPLICATIONS

- Car radio
- Car audio systems.

3 GENERAL DESCRIPTION

The SAA7707H performs all the signal functions in front of the power amplifiers and behind the AM and FMMPX demodulation of a car radio or the tape input.
These functions are:

- Interference absorption
- Stereo decoding
- RDS decoding
- FM and AM weak signal processing (soft mute, sliding stereo, etc.)
- Dolby-B tape noise reduction
- The audio controls (volume, balance, fader, tone and dynamics compression).

Some functions have been implemented in hardware (stereo decoder, RDS decoder and IAC) and are not freely programmable. Digital audio signals from external sources with I²S-bus formats are accepted. There are four independent analog output channels. This enables, in special system configurations, separate tone and equalization control for front and rear speakers.

The CDSP contains a basic program that enables a set with:

- AM/FM reception
- Sophisticated FM weak signal functions
- Music Search detection for Tape (MSS)
- Dolby-B tape noise reduction system
- CD play with compressor function
- Separate bass and treble tone control and fader/balance control.

For high-end sets with special and more sophisticated features, an additional Digital Signal Processor (DSP) can be connected. Examples of such features are:

- Noise-dependent volume control
- 10-band graphic equalizer
- Audio spectrum analyzer on display
- Signal delay for concert hall effects.

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DDD(tot)}$	total DC supply voltage	all supply pins	4.75	5	5.5	V
$I_{DDD(tot)}$	total DC supply current	maximum activity of the DSP; f_{xtal} = 36 MHz	–	160	200	mA
P_{tot}	total power dissipation	maximum activity of the DSP; f_{xtal} = 36 MHz	–	0.8	1.1	W
S/N	level ADC signal-to-noise ratio	RMS value; unweighted; B = 0 to 29 kHz; maximum input	48	54	–	dB
	ADC signal-to-noise ratio	not multiplexed; B = 19 kHz; V_i = 1 V (RMS)	81	85	–	dB
		multiplexed; unweighted; B = 19 kHz; 1 V (RMS)	72	76	–	dB
	ADC signal-to-noise ratio for FM-RDS	RMS value; B = 6 kHz; unweighted; f_c = 57 kHz	56	–	–	dB
V_{iFS}	ADC full-scale input voltage	V_{DDA1} = 4.75 to 5.5 V	$1.05V_{DDA1}$	$1.1V_{DDA1}$	$1.15V_{DDA1}$	V
THD	total harmonic distortion pins 62 and 71 to 75	f_i = 1 kHz; V_i = 1 V (RMS)	–	–71	–61	dB
			–	0.03	0.09	%
$V_{imc(rms)}$	maximum conversion input voltage level pins 62 and 71 to 75 (RMS value)	THD < 1%	1.1	–	–	V
RES	DAC resolution		–	18	–	bits
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio for DAC and operational amplifiers	R_L > 5 kΩ AC; R_{fb} = 2.7 kΩ; f_i = 1 kHz; R_{ref} = 18 kΩ; V_{oFS} = 2.8 V (p-p); maximum I^2S-bus signal	–	–70	–60	dB
DR	dynamic range of DAC	f_i = 1 kHz; –60 dB; A-weighted	92	102	–	dB
DS	digital silence of DAC	f_i = 20 Hz to 17 kHz; A-weighted	–	–110	–100	dB
$f_{xtalDSP}$	crystal frequency DSP part		–	36.86	–	MHz

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7707H	QFP80	plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 × 29 × 2.8 mm	SOT318-2

6 BLOCK DIAGRAM

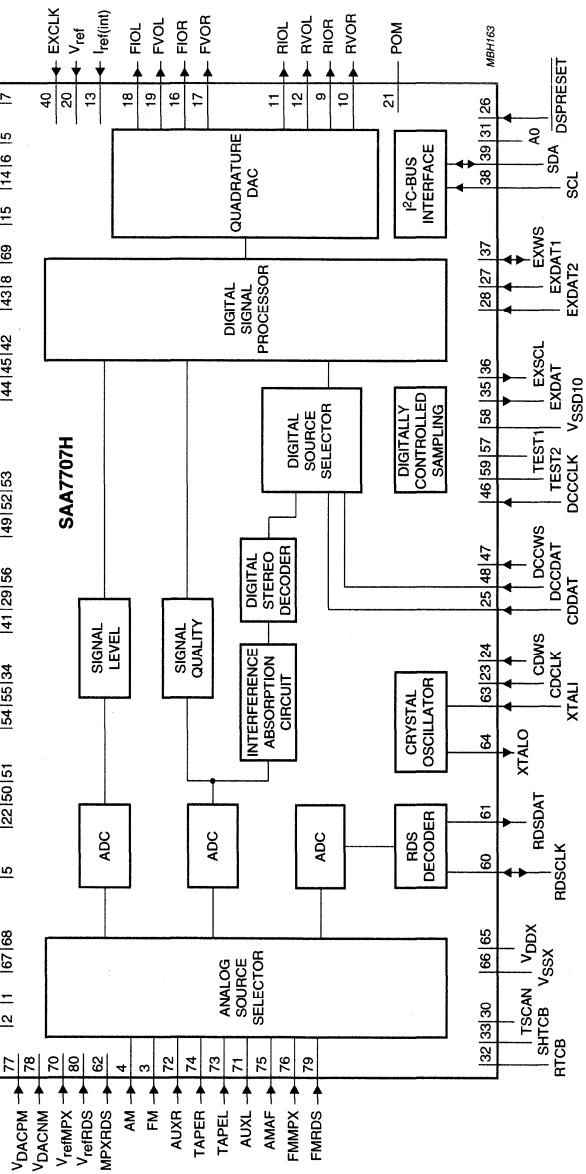


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	I/O	DESCRIPTION
V_{DACNL}	1	–	internal ground reference voltage for the level ADC
CINT	2		level ADC switch-mode integrator connector
FM	3	I	FM level input; via this pin, the level of the received FM radio signal is fed to the CDSP, the level information is required to enable correct functioning of the weak signal behaviour
AM	4	I	AM level input; via this pin, the level of the received AM radio signal is fed to the CDSP
V_{SSD1}	5	–	ground supply 1 for the DACs digital circuitry
V_{SSA}	6	–	ground supply for the DACs analog circuitry
V_{DDD1}	7	–	positive supply 1 for the DACs digital circuitry
V_{DDA}	8	–	positive supply for the DACs analog circuitry
RIOR	9	O	analog audio current output for rear right speaker
RVOR	10	O	analog audio voltage output for rear right speaker
RIOL	11	O	analog audio current output for rear left speaker
RVOL	12	O	analog audio voltage output for rear left speaker
$I_{ref(int)}$	13	I	internal reference current source input for the DACs
V_{SSO}	14	–	ground supply for DAC output operational amplifiers
V_{DDO}	15	–	positive supply for DAC output operational amplifiers
FIOR	16	O	analog audio current output for front right speaker
FVOR	17	O	analog audio voltage output for front right speaker
FIOL	18	O	analog audio current output for front left speaker
FVOL	19	O	analog audio voltage output for front left speaker
V_{ref}	20	I	voltage input for the internal reference buffer amplifier of the DAC
POM	21		activates the Power-on mute; timing is determined with an external capacitor
V_{SSD2}	22	–	ground supply 2 for the digital circuitry
CDCLK	23	I	clock input for CD digital audio source (I^2S-bus)
CDWS	24	I	Word Select input for CD digital audio source (I^2S-bus)
CDDAT	25	I	left/right data input for CD digital audio source (I^2S-bus)
$\overline{\text{DSPRESET}}$	26	I	input to reset DSP core (active LOW)
EXDAT1	27	I	external input data channel 1 (front) from extra DSP chip (I^2S-bus)
EXDAT2	28	I	external input data channel 2 (rear) from extra DSP chip (I^2S-bus)
V_{SSD9}	29	–	ground supply 9 for the digital circuitry
TSCAN	30		scan control (active HIGH)
A0	31		I^2S-bus selection for slave sub-address
RTCB	32		asynchronous reset test control block (active HIGH)
SHTCB	33		shift clock test control block (active HIGH)
V_{SSD7}	34	–	ground supply 7 for the digital circuitry
EXDAT	35	O	output data for extra external DSP chip (I^2S-bus)
EXSCL	36	O	output clock for extra external DSP chip (I^2S-bus)
EXWS	37	I/O	word select input/output for extra external DSP chip (I^2S-bus)

SYMBOL	PIN	I/O	DESCRIPTION
SCL	38	I	serial clock input (I^2C-bus)
SDA	39	I/O	serial data input/output (I^2C-bus)
EXCLK	40	I	external reference clock input to generate $4f_{as}$ and f_{as} synchronization; to be used if the I^2S-bus inputs are not suitable
V_{SSD8}	41	–	ground supply 8 for the digital circuitry
STEREO	42		FM stereo indication (active HIGH)
MSS/P	43		FM pause detector/MSS detector (active HIGH); also for IAC trigger output
$\overline{MUTE}$	44	I	MUTE input pin (active LOW); only for FM mode
DEEM	45		de-emphasis; CD and DCC (active HIGH) (I^2S-bus)
DCCCLK	46	I	DCC digital audio source clock input (I^2S-bus)
DCCWS	47	I	DCC digital audio source Word Select input (I^2S-bus)
DCCDAT	48	I	DCC digital audio source left/right data input (I^2S-bus)
V_{DDD3}	49	–	positive supply 3 for the digital circuitry
V_{SSD3}	50	–	ground supply 3 for the digital circuitry
V_{SSD4}	51	–	ground supply 4 for the digital circuitry
V_{DDD4}	52	–	positive supply 4 for the digital circuitry
V_{DDD5}	53	–	positive supply 5 for the digital circuitry
V_{SSD5}	54	–	ground supply 5 for the digital circuitry
V_{SSD6}	55	–	ground supply 6 for the digital circuitry
V_{DDD2}	56	–	positive supply 2 for the digital circuitry
TEST1	57		test pin 1 (this pin should be left open-circuit)
V_{SSD10}	58	–	ground supply 10 for the digital circuitry
TEST2	59		test pin 2 (this pin should be left open-circuit)
RDSCLK	60	I/O	radio data system bit clock input/output
RDSDAT	61	O	radio data system data output
MPXRDS	62	I	in FM mode, selects between FMMPX and RDSMPX input signal to the MPX decimation filter
XTALI	63	I	crystal oscillator input; can also be used as forced input in slave mode
XTALO	64	O	crystal oscillator output
V_{DDX}	65	–	positive supply crystal circuitry
V_{SSX}	66	–	ground supply crystal circuitry
V_{SSG}	67	–	ground guards for ADCs
V_{SSA1}	68	–	analog ground supply for ADCs
V_{DDA1}	69	–	analog positive supply for ADCs
V_{refMPX}	70	I	common mode reference voltage input for MPX ADC and buffers
AUXL	71	I	analog input for auxiliary left signal
AUXR	72	I	analog input for auxiliary right signal
TAPEL	73	I	analog input for tape left signal
TAPER	74	I	analog input for tape right signal
AMAF	75	I	analog input for AM audio frequency
FMMPX	76	I	analog input for FM multiplex signal

SYMBOL	PIN	I/O	DESCRIPTION
V_{DACPM}	77	I	supply voltage for the DACs switch capacitor of the FMMPX ADC and FMRDS ADC
V_{DACNM}	78	I	ground supply for the DACs switch capacitor of the FMMPX ADC and FMRDS ADC
FMRDS	79	I	analog FMMPX input for RDS decoding
V_{refRDS}	80	I	common mode reference voltage input for RDS ADC, level ADC and buffers

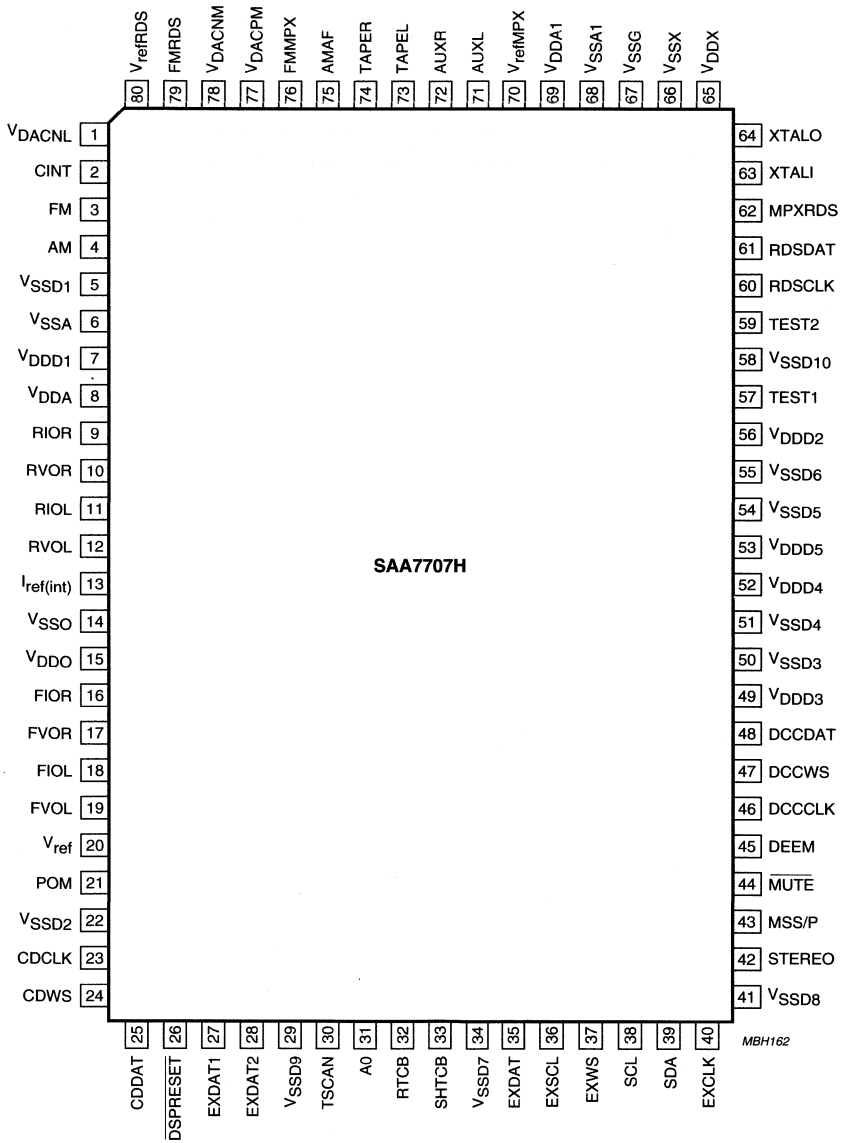


Fig.2 Pin configuration.

Dolby* Pro Logic Surround; Dolby 3 stereo; Incredible Sound

SAA7710T

FEATURES

- Two stereo I²S-bus digital input channels
- Three stereo I²S-bus digital output channels
- I²C-bus mode control
- Up to 45 ms on-chip delay-line (f_s = 44.1 kHz)
- Optional clock divider for crystal oscillator
- Package: SO32L
- Operating supply voltage range: 4.5 to 5.5 V.

Functions

- 4-channel active surround, 20 Hz to 20 kHz (maximum $\frac{1}{2}f_s$)
- Adaptive matrix
- 7 kHz low-pass filters
- Adjustable delay for surround channel
- Modified Dolby B noise reduction
- Noise sequencer
- Variable output matrix
- Sub woofer
- Centre mode control: on/off, normal, phantom, wide
- Output volume control
- Automatic balance and master level control with DC-offset filter
- Hall/matrix surround sound functions
- Incredible sound functions
- 3-band parametric equalizer on main channels left, centre, right (f_s = 44.1 kHz)
- 5-band parametric equalizer on main channels left, centre, right (f_s = 32 kHz)
- Tone control (bass/treble) on all four output channels (f_s = 44.1 kHz).

GENERAL DESCRIPTION

This data sheet describes the 104 ROM-code version of the SAA7710T chip. The SAA7710T chip is a high quality audio-performance digital add-on processor for digital sound systems. It provides all the necessary features for complete Dolby Pro Logic surround sound on chip.
In addition to the Dolby Pro Logic surround function, this device also incorporates a 3-band parametric equalizer, a 5-band parametric equalizer, a tone control section and a volume control. Instead of Dolby Pro Logic surround, the Hall/matrix surround and Incredible sound functions can be used together with the equalizer or tone control.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	DC supply voltage	−0.5	+6.5	V
ΔV_{DD}	voltage difference between two V_{DDx} pins	−	550	mV
V_i	maximum input voltage	−0.5	V_{DD} + 0.5	V
I_{DD}	DC supply current	−	50	mA
I_{SS}	DC supply current	−	50	mA
T_{amb}	ambient operating temperature	−40	+85	°C
T_{stg}	storage temperature range	−65	+150	°C

Remark Dolby*: Dolby' and 'Pro Logic' are trademarks of Dolby Laboratories Licensing Corporation. They are available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA94111, USA, from whom licensing and application information must be obtained.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7710T/N104	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

BLOCK DIAGRAM

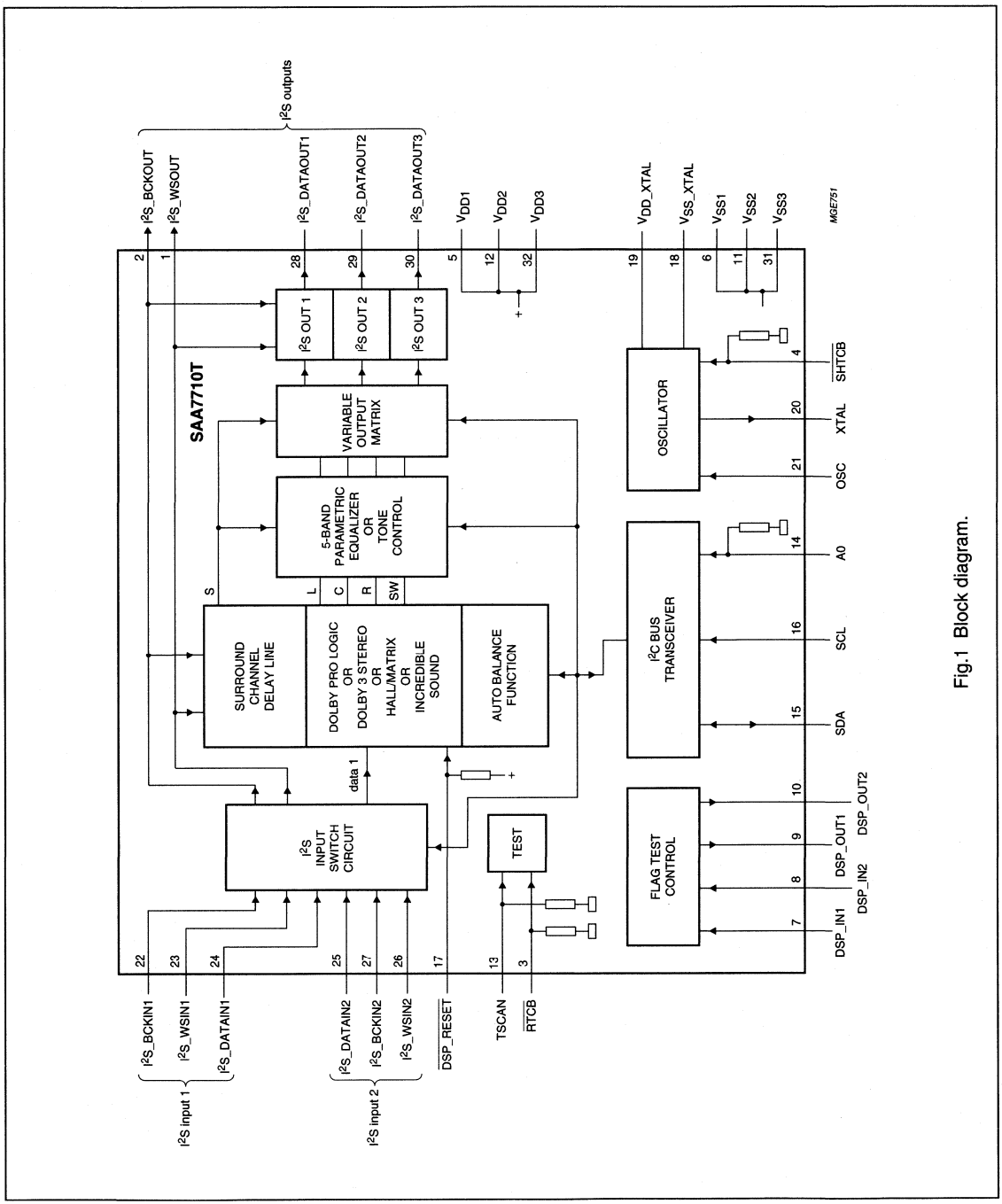


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
I²S_WSOUT	1	I²S-bus slave word-select output
I²S_BCKOUT	2	I²S-bus slave bit-clock output
$\overline{RTCB}$	3	asynchronous reset test control block input (active LOW)
$\overline{SHTCB}$	4	clock divider switch enable input (LOW = divide)
V_{DD1}	5	positive power supply
V_{SS1}	6	ground power supply
DSP_IN1	7	flag input 1
DSP_IN2	8	flag input 2
DSP_OUT1	9	flag output 1
DSP_OUT2	10	flag output 2
V_{SS2}	11	ground power supply
V_{DD2}	12	positive power supply
TSCAN	13	scan control input
A0	14	I²C-bus slave address selection input
SDA	15	I²C-bus serial data input/output
SCL	16	I²C-bus serial clock input
$\overline{DSP\_RESET}$	17	chip reset input (active LOW)
V_{SS_XTAL}	18	ground power supply crystal oscillator
V_{DD_XTAL}	19	positive power supply crystal oscillator
XTAL	20	crystal oscillator output
OSC	21	crystal oscillator input
I²S_BCKIN1	22	I²S-bus master bit-clock input 1
I²S_WSIN1	23	I²S-bus master word-select input 1
I²S_DATAIN1	24	I²S-bus master data input 1
I²S_DATAIN2	25	I²S-bus master data input 2
I²S_WSIN2	26	I²S-bus master word-select input 2
I²S_BCKIN2	27	I²S-bus master bit-clock input 2
I²S_DATAOUT1	28	I²S-bus slave data output 1
I²S_DATAOUT2	29	I²S-bus slave data output 2
I²S_DATAOUT3	30	I²S-bus slave data output 3
V_{SS3}	31	ground power supply
V_{DD3}	32	positive power supply

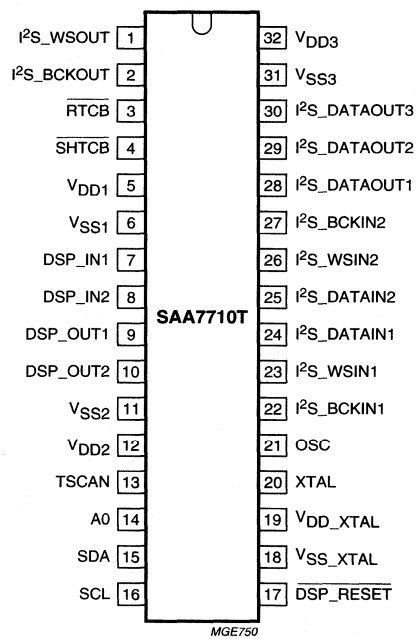


Fig.2 Pin configuration.

Digital Servo Driver 3 (DSD-3) SZA1010

FEATURES

Servo functions

- 1-bit class-D focus actuator driver (4 Ω)
- 1-bit class-D radial actuator driver (4 Ω)
- 1-bit class-D sledge motor driver (2 Ω).

Other features

- Supply voltage 5 V only
- Small package (SOT163-1)
- Higher efficiency, compared with conventional drivers, due to the class-D principle
- Built-in digital notch filters for higher efficiency
- Enable input for focus and radial driver
- Enable input for sledge driver
- 3-state input for radial driver
- Doubled clock frequency
- Differential outputs for all drivers
- Separate power supply pins for all drivers.

GENERAL DESCRIPTION

The SZA1010 or Digital Servo Driver 3 (DSD-3) consists of 1-bit class-D power drivers, which are specially designed for digital servo applications. Three such amplifiers are integrated in one chip, to drive the focus and radial actuators and the sledge motor of a compact disc optical system.

The main benefits of using this principle are its higher efficiency grade compared to conventional analog power amplifiers, its higher integration level, its differential output and the fact that only a few external components are needed. When using these digital power drivers in a digital servo application, the statement 'complete digital servo loop' becomes more realistic.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	4.5	–	5.5	V
$V_{DDA(F)}$	analog supply voltage focus actuator	4.5	–	5.5	V
$V_{DDA(R)}$	analog supply voltage radial actuator	4.5	–	5.5	V
$V_{DDA(S)}$	analog supply voltage sledge actuator	4.5	–	5.5	V
I_{DDDq}	quiescent digital supply current	–	–	10	μA
$I_{DDA(F)}$	analog supply current focus actuator	–	126	250	mA
$I_{DDA(R)}$	analog supply current radial actuator	–	20	250	mA
$I_{DDA(S)}$	analog supply current sledge actuator	–	150	560	mA
$f_{i(clk)}$	input clock frequency	–	8.4672	10	MHz
P_{tot}	total power dissipation	–	tbf	–	mW
T_{amb}	operating ambient temperature	−40	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SZA1010T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

BLOCK DIAGRAM

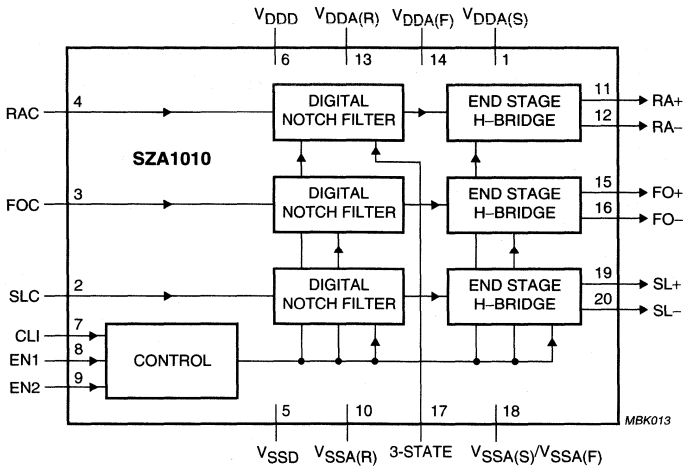


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{DDA(S)}$	1	analog supply voltage for sledge motor driver
SLC	2	PDM input for sledge driver
FOC	3	PDM input for focus driver
RAC	4	PDM input for radial driver
V_{SSD}	5	digital ground
V_{DDD}	6	digital supply voltage
CLI	7	clock input
EN1	8	enable input 1
EN2	9	enable input 2
$V_{SSA(R)}$	10	analog ground for radial driver
RA+	11	radial driver (positive output)
RA–	12	radial driver (negative output)
$V_{DDA(R)}$	13	analog supply voltage for radial driver
$V_{DDA(F)}$	14	analog supply voltage for focus
FO+	15	focus driver (positive output)
FO–	16	focus driver (negative output)
3-STATE	17	radial 3-state input
$V_{SSA(S)}$/ $V_{SSA(F)}$	18	analog ground for sledge driver/focus
SL+	19	sledge driver (positive output)
SL–	20	sledge driver (negative output)

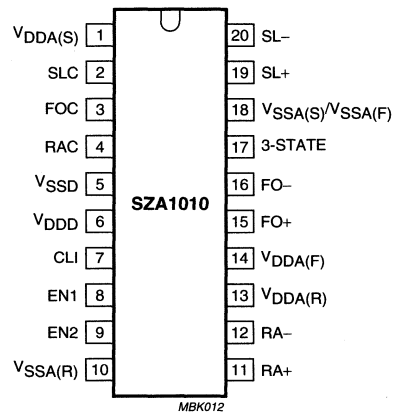


Fig.2 Pin configuration.

Photodetector amplifiers and laser supplies

TDA1300T; TDA1300TT

FEATURES

- Six input buffer amplifiers with low-pass filtering with virtually no offset
- HF data amplifier with a high or low gain mode
- Two built-in equalizers for single or double speed mode ensuring high playability in both modes
- Full automatic laser control including stabilization and an on/off switch and containing a separate supply V_{DDL} for power reduction
- Applicable with N-sub laser with N-sub or P-sub monitor diode
- Adjustable laser bandwidth and laser switch-on current slope
- Protection circuit preventing laser damage due to supply voltage dip
- Optimized interconnect between pick-up detector and TDA1301
- Wide supply voltage range
- Wide temperature range
- Low power consumption.

GENERAL DESCRIPTION

The TDA1300 is an integrated data amplifier and laser supply for three beam pick-up detectors applied in a wide range of mechanisms for Compact Disc (CD) and read only optical systems. It offers 6 amplifiers which amplify and filter the focus and radial diode signals adequately and provides an equalized RF signal for single or double speed mode which can be switched by means of the speed control pin.

The device can handle astigmatic, single Foucault and double Foucault detectors and is applicable with all N-sub lasers and N-sub or P-sub monitor diode units.

After a single initial adjustment the circuit keeps control over the laser diode current resulting in a constant light output power independent of ageing. The chip is mounted in a small SO24 or TSSOP24 package enabling mounting close to the laser pick-up unit on the sledge.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3	–	5.5	V
Diode current amplifiers (n = 1 to 6)						
$G_{d(n)}$	diode current gain		1.43	1.55	1.67	
$I_{O(d)}$	diode offset current		–	–	100	nA
B	3 dB bandwidth	$I_{i(d)}$ = 1.67 μA	50	–	–	kHz
RFE amplifier (built-in equalizer)						
$t_{d(eq)}$	equalization delay	f_i = 0.3 MHz	–	320	–	ns
$t_{d(f)}$	flatness delay	double speed	–	5	–	ns
Laser supply						
$I_{o(L)}$	output current	V_{DDL} = 3 V	–	–	−100	mA

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1300T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
TDA1300TT	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

BLOCK DIAGRAM

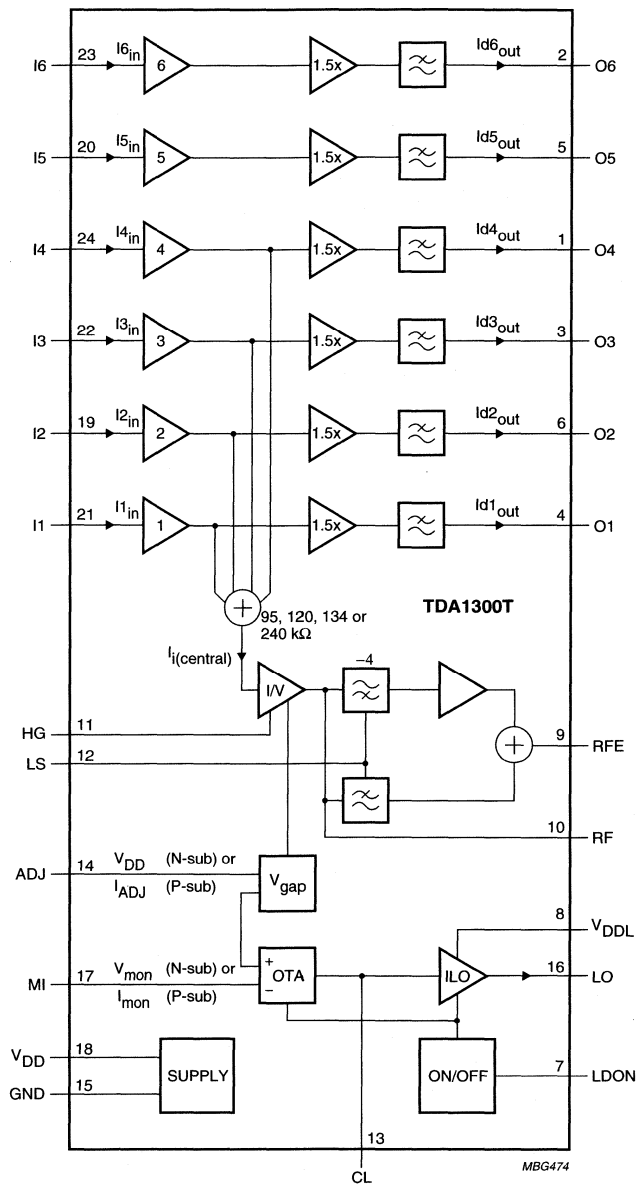


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
O4	1	current amplifier 4 output
O6	2	current amplifier 6 output
O3	3	current amplifier 3 output
O1	4	current amplifier 1 output
O5	5	current amplifier 5 output
O2	6	current amplifier 2 output
LDON	7	control pin for switching the laser on and off
V_{DDL}	8	laser supply voltage
RFE	9	equalized output voltage of sum signal of amplifiers 1 to 4
RF	10	unequalized output
HG	11	control pin for gain switch
LS	12	control pin for speed switch
CL	13	external capacitor
ADJ	14	P-sub monitor (if connected via resistor to GND); N-sub monitor (if connected to V_{DD})
GND	15	ground (substrate connection)
LO	16	laser output; current output
MI	17	monitor diode input (laser)
V_{DD}	18	supply
I2	19	photo detector input 2 (central)
I5	20	photo detector input 5 (satellite)
I1	21	photo detector input 1 (central)
I3	22	photo detector input 3 (central)
I6	23	photo detector input 6 (satellite)
I4	24	photo detector input 4 (central)

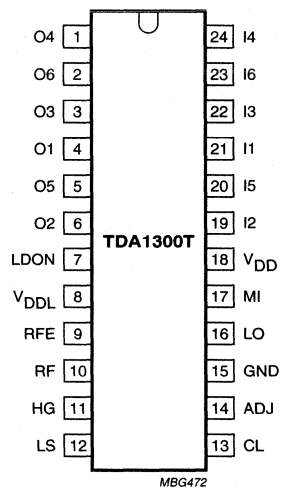


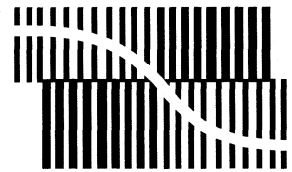
Fig.2 Pin configuration.

Low-voltage low-power stereo bitstream ADC/DAC

TDA1309H

FEATURES

- Low power
- Low supply voltage (2.7 V)
- Integrated high-pass filter to cancel DC offset (ADC)
- Analog loop-through function
- Multiple digital input/output formats possible
- $256f_s$ system clock frequency
- Several power-down modes
- Digital de-emphasis (DAC)
- Overload detector to enable automatic recording level adjustment (ADC)
- Input pads suitable for 5.5 V; low supply voltage interfacing
- High dynamic range
- DAC requires only one capacitor for post-filtering
- Small 44-pin quad flat pack with 0.8 mm pitch
- $256f_s$ system clock frequency in Analog-to-Digital (AD) and Digital-to-Analog (DA) mode
- Choice of three system clock frequencies ($192f_s$, $256f_s$ or $384f_s$) in DA mode.



BITSTREAM CONVERSION

APPLICATION

- Portable digital audio equipment.

GENERAL DESCRIPTION

The TDA1309H is a single chip stereo analog-to-digital and digital-to-analog converter employing bitstream conversion techniques. The low voltage requirement makes the device eminently suitable for use in low-voltage low-power portable digital audio equipment which incorporates recording and playback functions.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1309H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body $10 \times 10 \times 1.75$ mm	SOT307-2

QUICK REFERENCE DATA

$V_{DDD} = V_{DDA} = V_{DDO} = V_{DDD(F)} = 3$ V; $V_{SSD} = V_{SSA} = V_{SSO} = V_{SSD(F)} = 0$ V; $T_{amb} = 25$ °C; full scale sine wave input; mode 1; $f_i = 1$ kHz; 16-bit input data; conversion rate = 44.1 kHz; measurement bandwidth = 10 Hz to 20 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$V_{DDA(AD)}$	ADC analog supply voltage (pin 8)		2.7	3.0	4.0	V
$V_{DDA(DA)}$	DAC analog supply voltage (pin 25)		2.7	3.0	4.0	V
V_{DDO}	operational amplifiers supply voltage (pin 19)		2.7	3.0	4.0	V
V_{DDD}	ADC and DAC digital supply voltage (pin 28)		2.7	3.0	4.0	V
$V_{DDD(F)}$	digital filters supply voltage (pin 34)		2.7	3.0	4.0	V
$I_{DDA(AD)}$	ADC analog supply current (pin 8)		–	8	12.5	mA
$I_{DDA(DA)}$	DAC analog supply current (pin 25)		–	3.5	7	mA
I_{DDO}	operational amplifiers supply current (pin 19)		–	12	18	mA
I_{DDD}	ADC and DAC digital supply current (pin 28)		–	0.2	0.5	mA
$I_{DDD(F)}$	digital filters supply current (pin 34)		–	20	30	mA
$I_{PD(DA)}$	DAC power-down current		–	15	20	mA
$I_{PD(AD)}$	ADC power-down current		–	7	10	mA
T_{amb}	operating ambient temperature		–20	–	+75	°C
Analog-to-digital converter						
$V_{I(rms)}$	input voltage (RMS value)	note 1	–	0.5	0.54	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–85	–80	dB
		at –60 dB; A-weighted	–	–35	–30	dB
S/N	idle channel signal-to-noise ratio	$V_I = 0$ V; A-weighted	90	95	–	dB
α_{cs}	channel separation		–	90	–	dB
Digital-to-analog converter						
$V_{O(rms)}$	output voltage (RMS value)	note 2	0.43	0.5	0.57	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–90	–82	dB
		at –60 dB; A-weighted	–	–38	–34	dB
		at –60 dB; A-weighted; note 3	–	–44	–	dB
S/N	idle channel signal-to-noise ratio	code 0000H; A-weighted	–	104	–	dB
α_{cs}	channel separation		90	100	–	dB

Notes

1. The input voltage for full scale digital output is a function of $V_{DDA(AD)}$.
2. At full scale digital input; no de-emphasis; $V_{O(rms)}$ is a function of $V_{DDA(DA)}$.
3. 18-bit input data.

BLOCK DIAGRAM

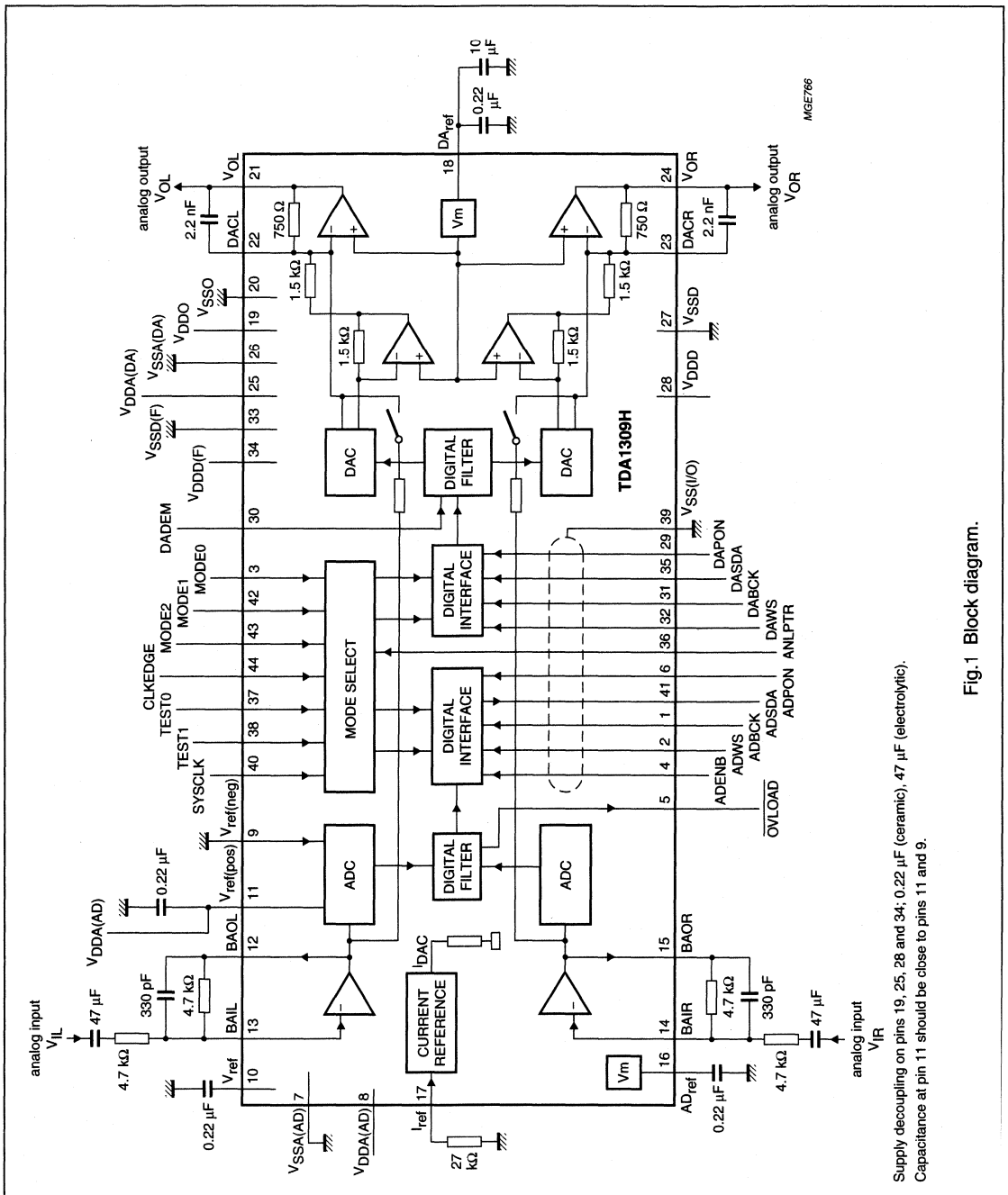


Fig.1 Block diagram.

Supply decoupling on pins 19, 25, 28 and 34; 0.22 µF (ceramic), 47 µF (electrolytic).
Capacitance at pin 11 should be close to pins 11 and 9.

PINNING

SYMBOL	PIN	DESCRIPTION
ADBCK	1	ADC input bit clock; $32f_s$ or $64f_s$
ADWS	2	ADC word select input at f_s
MODE0	3	ADC/DAC mode select input
ADENB	4	ADC serial data enable input (active HIGH)
$\overline{\text{OVLOAD}}$	5	ADC output overload flag (active LOW)
ADPON	6	ADC power-on-mode input (active HIGH)
$V_{SSA(AD)}$	7	ADC analog ground supply voltage
$V_{DDA(AD)}$	8	ADC analog supply voltage
$V_{ref(neg)}$	9	ADC negative reference voltage input (ground)
V_{ref}	10	ADC decoupling capacitor
$V_{ref(pos)}$	11	ADC positive reference voltage decoupling capacitor
BAOL	12	ADC input amplifier output left
BAIL	13	ADC input amplifier virtual ground left
BAIR	14	ADC input amplifier virtual ground right
BAOR	15	ADC input amplifier output right
AD_{ref}	16	ADC decoupling capacitor
I_{ref}	17	ADC/DAC reference current resistor input
DA_{ref}	18	DAC decoupling capacitor
V_{DDO}	19	ADC/DAC operational amplifier supply voltage
V_{SSO}	20	ADC/DAC operational amplifier ground supply voltage
V_{OL}	21	DAC output voltage left
DACL	22	DAC output current left
DACR	23	DAC output current right
V_{OR}	24	DAC output voltage right
$V_{DDA(DA)}$	25	DAC analog supply voltage
$V_{SSA(DA)}$	26	DAC analog ground supply voltage
V_{SSD}	27	ADC/DAC digital ground supply voltage
V_{DDD}	28	ADC/DAC digital supply voltage
DAPON	29	DAC power-on-mode input (active HIGH)
DADEM	30	DAC digital de-emphasis input (active HIGH)
DABCK	31	DAC input bit clock; $32f_s$, $48f_s$ or $64f_s$
DAWS	32	DAC word select input at f_s
$V_{SSD(F)}$	33	ADC/DAC digital filters ground supply voltage
$V_{DDD(F)}$	34	ADC/DAC digital filters supply voltage
DASDA	35	DAC serial data input
ANLPTR	36	ADC/DAC analog loop-through input (active HIGH)
TEST0	37	ADC/DAC enable test mode 0 input (LOW is normal mode)
TEST1	38	ADC/DAC enable test mode 1 input (LOW is normal mode)
$V_{SS(I/O)}$	39	ADC/DAC digital input/output ground supply voltage
SYSCLK	40	ADC/DAC system clock input ($f_{sys} = 256f_s$; DAC also $192f_s$ and $384f_s$)

SYMBOL	PIN	DESCRIPTION
ADSDA	41	ADC serial data output
MODE1	42	ADC/DAC mode 1 select input
MODE2	43	ADC/DAC mode 2 select input
CLKEDGE	44	ADC/DAC input bit clock rising/falling edge

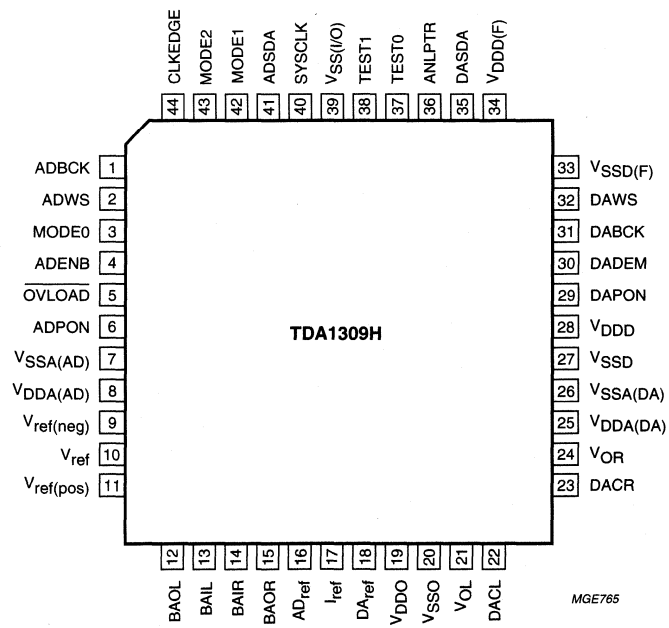
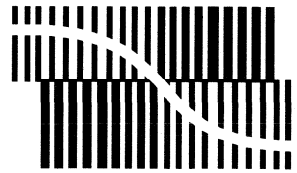


Fig.2 Pin configuration.

General Digital Input (GDIN) TDA1373H

FEATURES

- Four operating modes:
  - Sample Rate Conversion (SRC) mode
  - AD/DA mode
  - SLAVE-VCO mode
  - SLAVE-VCXO mode
- Full digital sample rate conversion over a wide range of input sample rates
- Fast and automatic detection and locking to the input sample rate with continuous tracking
- Digital Phase-Locked Loop (PLL) with adaptive bandwidth which removes jitter on the digital audio input
- Audio outputs (soft) muted during loop acquisition
- Full linear phase processing based on all-FIR filtering
- Integrated full digital IEC 958 demodulator for digital input signals (AES/EBU or SPDIF format) with intelligent error handling
- Extended input sample frequency range
- IEC 958 Channel Status (CS) and User Channel (UC) outputs
- On-chip CS and/or UC demodulation and buffering (consumer and professional format)
- Dedicated subcode processing for Compact Disc (CD)
- Final output quantization to 16, 18 or 20 bits with optional in-audio-band noise shaping
- Bitstream input and output for coupling with 1-bit analog-to-digital conversion (ADC) and digital-to-analog conversion (DAC)
- I^2S and Japanese serial input formats supported for SRC and DAC functions
- I^2S and Japanese serial output formats supported for SRC and ADC functions
- I^2S and Japanese 4× oversampled serial output available for SRC and ADC functions
- 8-bit digital gain/attenuation control
- Switchable Digital Signal Processor (DSP)-interface (I^2S input and output) for additional audio processing
- Additional clock outputs available at 768, 384, 256 and $128f_{so}$
- 3-line serial microcontroller interface, compatible with the Philips CD I.C. protocol (HCL)



BITSTREAM CONVERSION

- 5 V power supply
- 0.7 µm double metal Complementary Metal Oxide Semiconductor (CMOS)
- SRC THD + N:
  - −113 dB over the 0 to 20 kHz band (1 kHz, 20 bits input and output) (see Fig.3)
  - −95 dB over the 0 to 20 kHz band (1 kHz, 16 bits input and output)
- Pass band ripple smaller than ±0.004 dB for up-sampling and down-sampling filters
- Stop band suppression:
  - selectable between 70 dB and 50 dB for 64× up-sampling filters
  - 80 dB for 128× down-sampling filters
- Microcontroller operated and stand-alone mode.

APPLICATIONS

- Professional audio equipment for:
  - mixing
  - recording
  - editing
  - broadcasting
- CD-Recordable (CD-R)
- Digital Speaker Systems (DSS)
- Digital Compact Cassette recorders (DCC)
- Digital Audio Tape (DAT) and MD recorders
- Digital amplifiers
- Jitter killers.

General Digital Input (GDIN) TDA1373H

GENERAL DESCRIPTION

The TDA1373H is a General Digital Input (GDIN) device for audio signals which is able to perform a high-quality sample rate conversion of digital audio signals (**SRC mode**). The device reads several serial input formats and signals in the IEC 958 digital audio format (also known as AES/EBU or SPDIF signals). For this purpose a full Audio Digital Input Circuit (ADIC) is present in the device.

An internal digital PLL results in extensive jitter removal from incoming digital audio signals without any analog loop electronics. The standard 20 bit output word length can be limited to 16 or 18 bits by means of 'in-audio-band noise shaping'.

The GDIN digital filters can also be reused for Bitstream ADC and DAC conversion (**AD/DA mode**). The internal digital PLL can be reconfigured to operate the GDIN in a slave mode, where the output sample frequency of the device is locked to the incoming sample rate (**SLAVE-VCO** and **SLAVE-VCXO** modes).

The combination of an ADIC function, sample rate conversion and Bitstream ADC and DAC results in a device with a highly versatile functionality and large replacement value in consumer and professional audio sets.

QUICK REFERENCE DATA

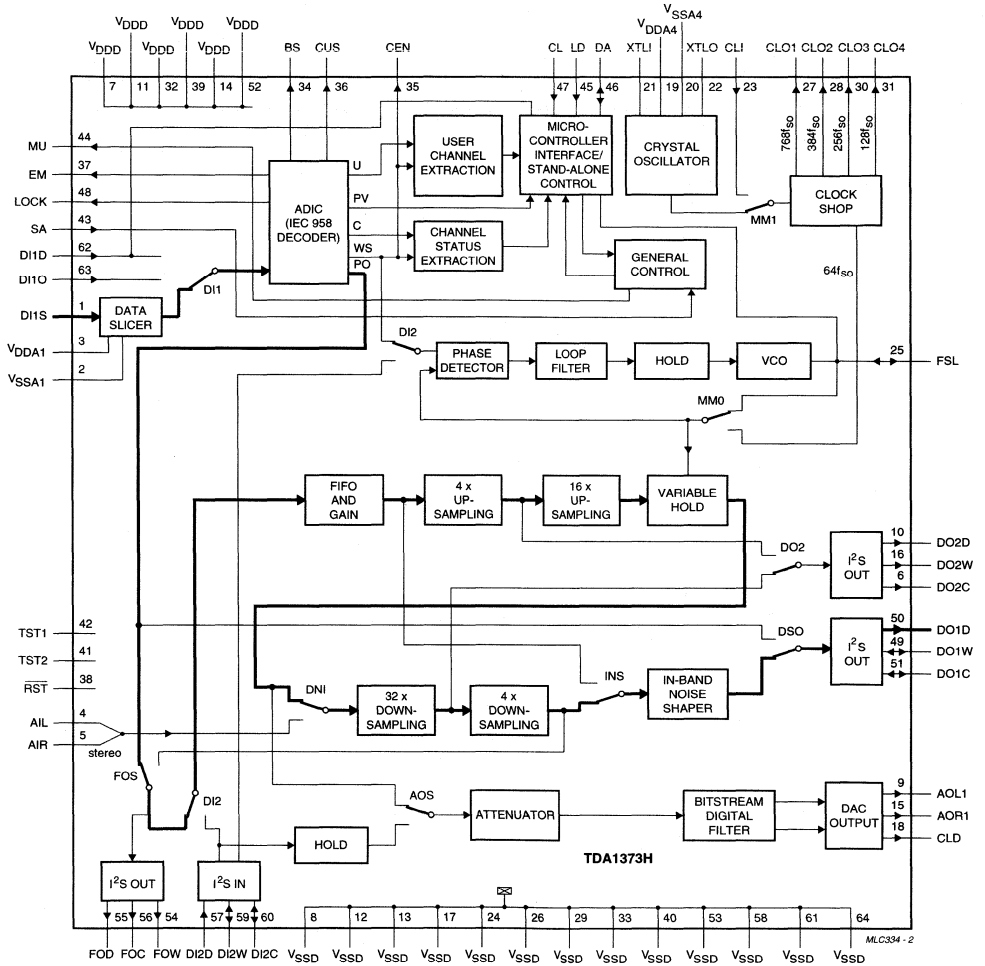
All inputs and outputs CMOS compatible; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	$f_{so} > 44.1$ kHz	4.75	5	5.5	V
		$f_{so} \leq 44.1$ kHz	4.5	5	5.5	V
$I_{DD(tot)}$	total supply current	$f_{so} = 44.1$ kHz	–	155	–	mA
P_{tot}	total power dissipation	$f_{so} = 44.1$ kHz	–	775	–	mW
		$f_{so} = 49$ kHz; $V_{DD} = 5.5$ V	–	1030	–	mW
IEC 958 input DI1S (high-sensitivity IEC input)						
$V_{i(p-p)}$	AC input voltage (peak-to-peak value)		0.2	–	V_{DD}	V
Clock and timing						
$f_{so(max)}$	maximum output sample frequency	$V_{DD} = 4.75$ V	49	55	–	kHz
Temperature						
T_{amb}	operating ambient temperature		0		70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1373H	QFP64	Plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.7 mm; high stand-off height	SOT319-1

BLOCK DIAGRAM



Switches MM1 and MM0 are controlled indirectly via the mode selection. All other switches can be controlled directly by the user.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION	TYPE
DI1S	1	IEC 958 digital audio input 'S' (200 mV peak-to-peak value)	E036A
V_{SSA1}	2	IEC 958 slicer analog ground	E038A
V_{DDA1}	3	IEC 958 slicer analog supply voltage	E037A
AIL	4	Bitstream audio input left	HPP01
AIR	5	Bitstream audio input right	HPP01
DO2C	6	serial digital audio output 2; bit clock output ($192f_{so}$)	OPF40
V_{DDD}	7	digital supply voltage; note 1	–
V_{SSD}	8	digital ground; note 2	–
AOL1	9	Bitstream audio output left	OPF40
DO2D	10	DLO = 0; serial digital audio output 2; data; DLO = 1; Bitstream audio output left inverted ($\overline{AOL1}$); note 3	OPF40
V_{DDD}	11	digital supply voltage; note 1	–
V_{SSD}	12	digital ground; note 2	–
V_{SSD}	13	digital ground; note 2	–
V_{DDD}	14	digital supply voltage; note 1	–
AOR1	15	Bitstream audio output right	OPF40
DO2W	16	DLO = 0; serial digital audio output 2; word select output ($4f_{so}$); DLO = 1; Bitstream audio output right inverted ($\overline{AOR1}$); note 3	OPF40
V_{SSD}	17	digital ground; note 2	–
CLD	18	Bitstream DAC clock (192 or $128f_{so}$)	OPF43
V_{DDA4}	19	oscillator analog supply voltage	E037A
V_{SSA4}	20	oscillator analog ground	E038A
XTLI	21	crystal input $768f_{so}$	OSX01
XTLO	22	crystal output	OSX01
CLI	23	external VCO input (SLAVE-VCO mode only)	HPP01
V_{SSD}	24	digital ground; note 2	–
FSL	25	SA = 0 (microcontroller operated) external VCO output (slave modes only); SA = 1 (stand-alone control) DI11 control line; note 4	HOF21
V_{SSD}	26	digital ground; note 2	–
CLO1	27	clock output $768f_{so}$	OPF40
CLO2	28	clock output $384f_{so}$	OPF40
V_{SSD}	29	digital ground; note 2	–
CLO3	30	clock output $256f_{so}$	OPF40
CLO4	31	clock output $128f_{so}$;	OPF40
V_{DDD}	32	digital supply voltage; note 1	–
V_{SSD}	33	digital ground; note 2	–
BS	34	block sync; channel status/user channel/CD subcode	OPF40
CEN	35	data enable; channel status/user channel/CD subcode	OPF40
CUS	36	data bit; channel status/user channel/CD subcode	OPF40
EM	37	IEC 958 source pre-emphasis flag	OPF20

SYMBOL	PIN	DESCRIPTION	TYPE
$\overline{RST}$	38	power-on reset input (active LOW)	HPP07
V_{DDD}	39	digital supply voltage; note 1	–
V_{SSD}	40	digital ground; note 2	–
TST2	41	test pin 2 (LOW for normal operation)	HPP01
TST1	42	test pin 1 (LOW for normal operation)	HPP01
SA	43	Stand-alone/microcontroller operated selection; SA = 1 for stand-alone operation	HPP01
MU	44	mute flag (active HIGH)	OPF40
LD	45	SA = 0 (microcontroller operated) microcontroller interface; load (read/write); SA = 1 (stand-alone control) NSD control line; note 4	HPP01
DA	46	SA = 0 (microcontroller operated) microcontroller interface (data); SA = 1 (stand-alone control) DI2 control line; note 4	HOF41
CL	47	SA = 0 (microcontroller operated) microcontroller interface (clock); SA = 1 (stand-alone control) QU1/QU0 control line; note 4	HPP01
LOCK	48	ADIC lock flag (active HIGH)	OPF40
DO1W	49	serial digital audio output 1; word select input/output (f_{so})	HOF41
DO1D	50	serial digital audio output 1; data	OPF43
DO1C	51	serial digital audio output 1; bit clock input/output ($48f_{so}$)	HOF41
V_{DDD}	52	digital supply voltage; note 1	–
V_{SSD}	53	digital ground; note 2	–
FOW	54	serial digital audio feature output; word select	OPF43
FOD	55	serial digital audio feature output; data	OPF43
FOC	56	serial digital audio feature output; bit clock ($64f_{so}$)	OPF43
DI2D	57	serial digital audio input 2; data	HPP01
V_{SSD}	58	digital ground; note 2	–
DI2W	59	serial digital audio input 2; word select	HOF21
DI2C	60	serial digital audio input 2; bit clock output	HOF21
V_{SSD}	61	digital ground; note 2	–
DI1D	62	SA = 0 (microcontroller operated) IEC 958 digital audio input 'D' (CMOS level); SA = 1 (stand-alone control) MSO control line; note 4	HPP01
DI1O	63	IEC 958 digital audio input 'O' (CMOS level)	HPP01
V_{SSD}	64	digital ground; note 2	–

Notes

1. All V_{DDD} pins are internally connected.
2. All V_{SSD} pins are internally connected.
3. DLO is a command flag from register 4 (see Section "Command registers").
4. SA is the stand-alone/microcontroller operated pin (pin 43). DI11, NSD, DI2, QU1, QU0 and MS0 are command flags to control the operation of the device. For more information see Section "Controlling the GDIN".

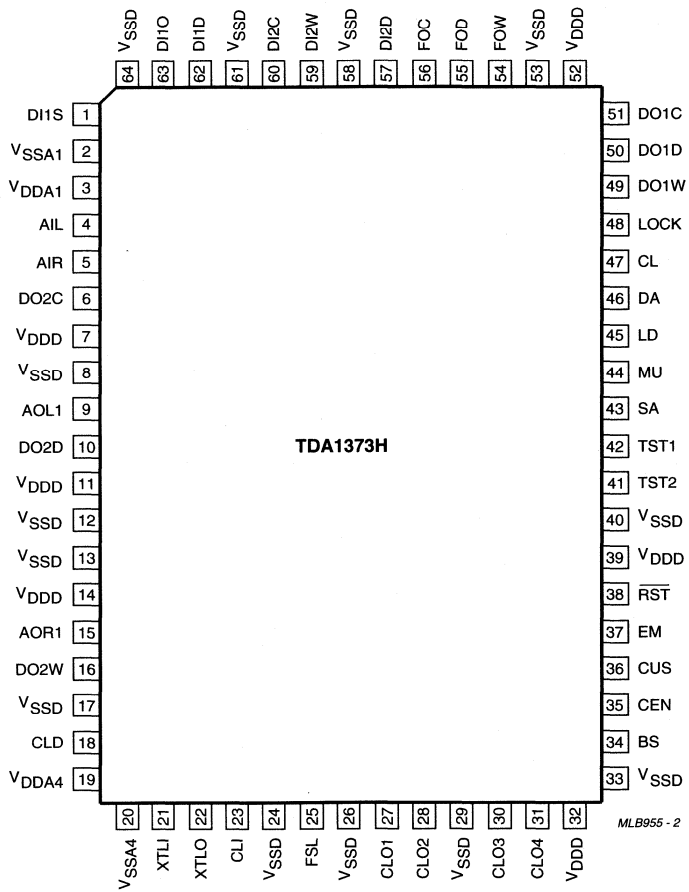


Fig.2 Pin configuration.

40 W car radio high power amplifier TDA1560Q

FEATURES

- Very high output power
- Low power dissipation when used for music signals
- Switches to low output power in the event of excessive heatsink temperatures
- Requires few external components
- Fixed gain
- Low cross-over distortion
- No switch-on/switch-off plops
- Mode select switch
- Low offset voltage at the output
- Load dump protection
- Short-circuit safe to ground, V_P and across load
- Protected against electrostatic discharge
- Thermally protected
- Diagnostic facility
- Flexible leads.

GENERAL DESCRIPTION

The TDA1560Q is an integrated Bridge-Tied Load (BTL) class-H high power amplifier. In a load of 8 Ω, the output power is 40 W typical at a THD of 10%.

The encapsulation is a 17-lead DIL-bent-SIL plastic power package. The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	operating	8.0	14.4	18	V
		non-operating	–	–	30	V
		load dump protected	–	–	45	V
I_{ORM}	repetitive peak output current		–	–	4	A
$I_{q(tot)}$	total quiescent current		–	100	160	mA
I_{sb}	standby current		–	5	50	μA
G_v	voltage gain		29	30	31	dB
P_o	output power	R_L = 8 Ω; THD = 10%	–	40	–	W
		R_L = 8 Ω; THD = 0.5%	–	30	–	W
SVRR	supply voltage ripple rejection	f_i = 100 Hz to 10 kHz; R_S = 0 Ω	48	55	–	dB
V_{no}	noise output voltage		–	100	300	μV
$\|Z_i\|$	input impedance		180	300	–	kΩ
$\|\Delta V_O\|$	DC output offset voltage		–	–	150	mV

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1560Q	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1

BLOCK DIAGRAM

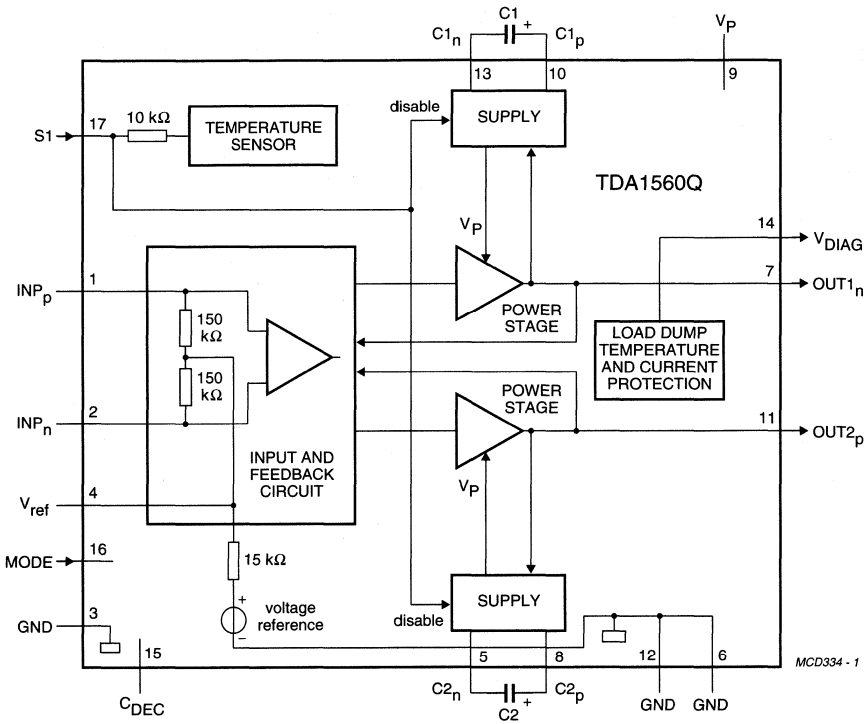


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
INP_p	1	positive input
INP_n	2	negative input
GND	3	ground
V_{ref}	4	reference voltage
$C2_n$	5	capacitor C2 negative terminal
GND	6	ground
$OUT1_n$	7	output 1 (negative)
$C2_p$	8	capacitor C2 positive terminal
V_P	9	supply voltage
$C1_p$	10	capacitor C1 positive terminal
$OUT2_p$	11	output 2 (positive)
GND	12	ground
$C1_n$	13	capacitor C1 negative terminal
V_{DIAG}	14	diagnostic voltage output
C_{DEC}	15	decoupling
MODE	16	mode select switch input
S1	17	class-B/class-H input switch

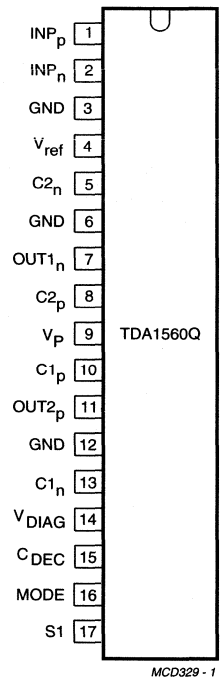


Fig.2 Pin configuration.

2 × 23 W high efficiency car radio power amplifier

TDA1561Q

FEATURES

- Low dissipation due to switching from Single-Ended (SE) to Bridge-Tied Load (BTL) mode
- High Common Mode Rejection Ratio (CMRR)
- Mute/standby/operating/SE-only (mode select pin)
- Zero crossing mute and standby circuit
- Load dump protection circuit
- Short-circuit safe to ground, to supply voltage and across load
- Loudspeaker protection circuit
- Device switches to single-ended operation at excessive junction temperatures.

GENERAL DESCRIPTION

The TDA1561Q is a monolithic power amplifier in a 13 lead single-in-line (SIL) plastic power package. It contains two identical 23 W amplifiers. The dissipation is minimized by switching from SE to BTL mode, only when a higher output voltage swing is needed. The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	DC biased	6.0	14.4	18	V
		non operating	–	–	30	V
		load dump	–	–	50	V
I_{ORM}	repetitive peak output current		–	–	4	A
$I_{q(tot)}$	total quiescent current	$R_L = \infty$	–	95	150	mA
I_{stb}	standby current		–	1	50	μA
$\lvert Z_i \rvert$	input impedance		–	60	–	kΩ
P_o	output power	RL = 4 Ω; EIAJ	–	36	–	W
		THD 10%	21	23	–	W
G_v	voltage gain		31	32	33	dB
CMRR	common mode rejection ratio	f = 1 kHz; R_s = 0 Ω	–	80	–	dB
SVRR	supply voltage ripple rejection	f = 1 kHz; R_s = 0 Ω	45	55	–	dB
$\lvert \Delta V_O \rvert$	DC output offset voltage		–	–	150	mV
α_{cs}	channel separation	R_s = 0 kΩ	40	60	–	dB
$\lvert \Delta G_v \rvert$	channel unbalance		–	–	1	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1561Q	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6

BLOCK DIAGRAM

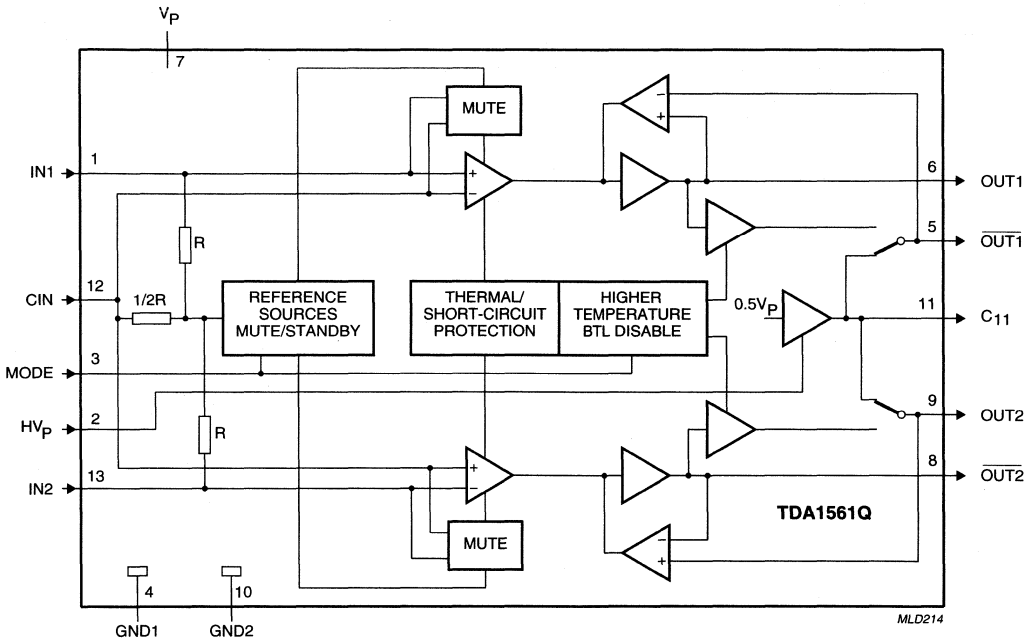


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
IN1	1	input 1
HV_P	2	half supply voltage control input
MODE	3	mute/standby/operating/SE-only
GND1	4	ground 1
$\overline{OUT1}$	5	inverting output 1
OUT1	6	non-inverting output 1
V_P	7	supply voltage
$\overline{OUT2}$	8	inverting output 2
OUT2	9	non-inverting output 2
GND2	10	ground 2
C_{11}	11	electrolytic capacitor for single-ended (SE) mode
CIN	12	common input
IN2	13	input 2

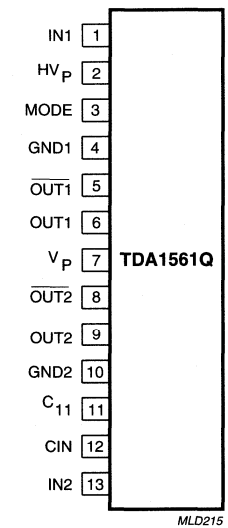


Fig.2 Pin configuration.

Multiple output voltage regulators

TDA3601Q
TDA3601AQ

FEATURES

- Six fixed voltage regulators
- Three microprocessor-controlled regulators
- Two V_P-state controlled regulators
- One fixed voltage regulator (can operate during load dump or thermal shutdown)
- V_{P1} supply pin (low current pin)
- V_{P2} supply pin (high current pin)
- RESET output (TDA3601Q) or $\overline{\text{RESET}}$ output (TDA3601AQ)
- Internally fixed timer of 100 μs
- Externally fixed delay timer
- High ripple rejection
- Flexible leads.

PROTECTION

- Current limit protection for regulator 1
- Foldback current limit protection (regulators 2 to 6)
- Load dump protection
- Thermal protection
- Regulator outputs DC short-circuit-safe to ground, V_P and other regulator outputs
- Capable of handling high energy on any of the output pins
- Reverse polarity safe.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Entire device						
V_{P1}	supply voltage range	operating	11	13.2	18	V
		load dump; notes 1 and 2	–	–	50	V
V_{P2}	supply voltage range	operating	11	13.2	18	V
		non-operating	–	–	30	V
		load dump; note 1	–	–	50	V
$I1_{tot}$	total quiescent current, V_{P1}	V_{P2} = 0; note 3	–	1	1.4	mA
T_c	crystal temperature		–	–	150	°C
Voltage regulators						
V_{R1}	output voltage regulator 1	0.5 mA ≤ I_{R1} ≤ 20 mA	4.75	5	5.25	V
V_{R2}	output voltage regulator 2	5 mA ≤ I_{R2} ≤ 200 mA	1.9	2.1	2.3	V
V_{R3}	output voltage regulator 3	5 mA ≤ I_{R3} ≤ 150 mA	4.75	5	5.25	V
V_{R4}	output voltage regulator 4	5 mA ≤ I_{R4} ≤ 150 mA	9	9.5	10	V
V_{R5}	output voltage regulator 5	5 mA ≤ I_{R5} ≤ 200 mA	9	9.5	10	V
V_{R6}	output voltage regulator 6	5 mA ≤ I_{R6} ≤ 200 mA	9.3	9.75	10.2	V

Notes

1. Load dump, during 50 ms, t_r > 2.5 ms.
2. Regulator 1 operating, 0.5 mA ≤ I_{R1} ≤ 20 mA.
3. V_{P1} = 13.2 V; V_{P2} = R4-sel = R5-sel = 0; I_{R1} = 0.

BLOCK DIAGRAM

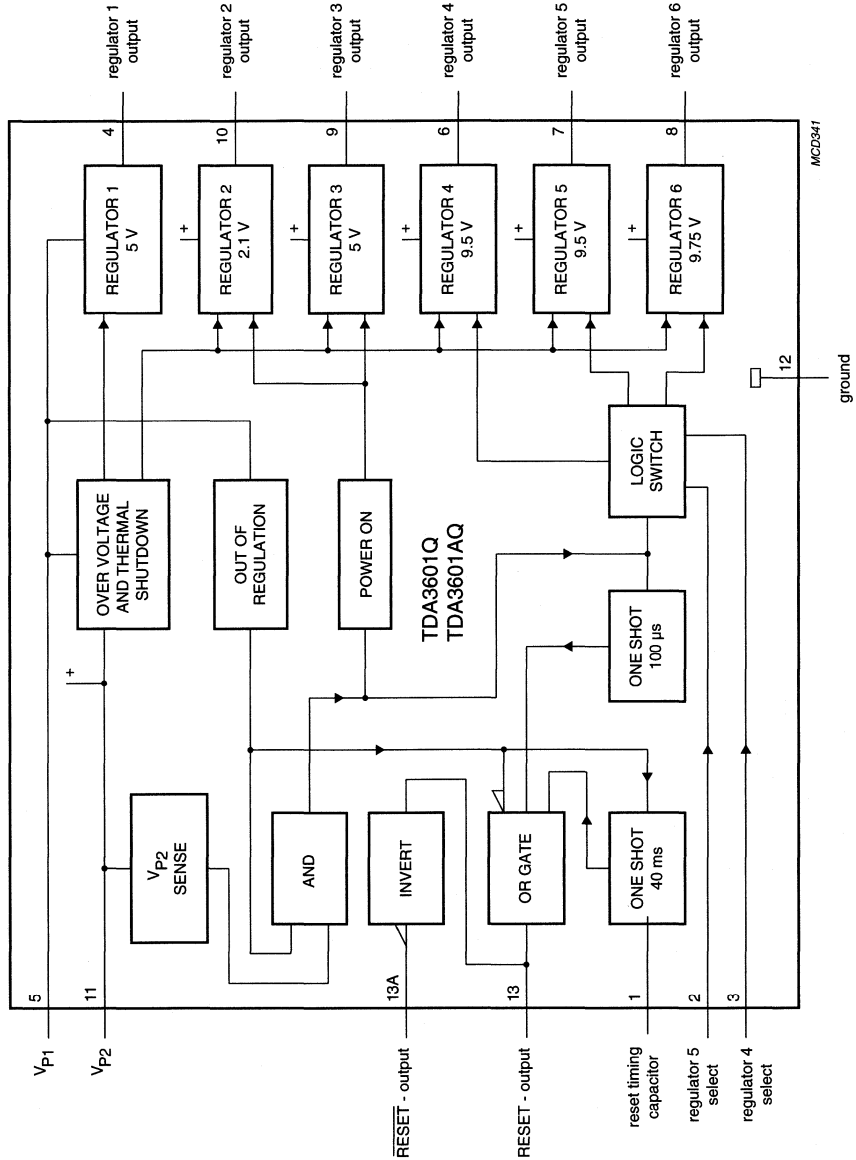


Fig.1 Block diagram.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA3601Q	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6
TDA3601AQ			

GENERAL DESCRIPTION

The circuit contains five fixed voltage regulators with foldback current protection and one fixed voltage regulator (REGULATOR 1) that also operates during a load dump. In addition, a RESET function (TDA3601Q) or $\overline{\text{RESET}}$ function (TDA3601AQ), timer functions and a logic multiplexer are implemented.

PINNING

SYMBOL	PIN	DESCRIPTION
C_{RESET}	1	reset timing capacitor
R5-sel	2	regulator 5 select
R4-sel	3	regulator 4 select
REG1	4	regulator 1 output (5 V)
V_{P1}	5	supply voltage
REG4	6	regulator 4 output (9.5 V)
REG5	7	regulator 5 output (9.5 V)
REG6	8	regulator 6 output (9.75 V)
REG3	9	regulator 3 output (5 V)
REG2	10	regulator 2 output (2.4 V)
V_{P2}	11	supply voltage
GND	12	ground
RES	13	RESET output (TDA3601Q)
$\overline{\text{RES}}$	13A	$\overline{\text{RESET}}$ output (TDA3601AQ)

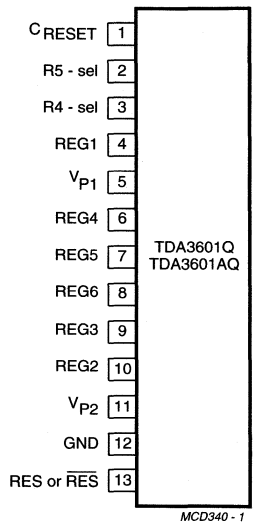


Fig.2 Pin configuration.

Multiple voltage regulator with switch TDA3605Q

FEATURES

- Two V_P-state controlled regulators (regulator 1 and regulator 3) and a power switch
- Regulator 2, reset and ignition buffer operates during load dump and thermal shutdown
- Separate control pins for switching regulator 1, regulator 3 and the power switch
- Supply voltage range of −18 to +50 V (operating from 11 V)
- Low reverse current of regulator 2
- Low quiescent current (when regulator 1, regulator 3, and power switch are switched off)
- Hold output (only valid when regulator 1 is switched on)
- Reset and hold outputs (open collector outputs)
- Adjustable reset delay time
- High ripple rejection
- Back-up capacitor for regulator 2.

PROTECTIONS

- Reverse polarity safe (down to −18 V without high reverse current)
- Able to withstand voltages up to 18 V at the outputs (supply line may be short-circuited)
- ESD protected on all pins
- Thermal protection
- Local thermal protection for power switch
- Load dump protection
- Foldback current limit protection for regulators 1, 2 and 3
- Delayed second current limit protection for the power switch (at short-circuit)
- The regulator outputs and the power switch are DC short-circuited safe to ground and V_P.

GENERAL DESCRIPTION

The TDA3605Q is a multiple output voltage regulator with a power switch, intended for use in car radios with or without a microcontroller. It contains:

1. Two fixed voltage regulators with a foldback current protection (regulator 1 and regulator 3) and one fixed voltage regulator (regulator 2), intended to supply a microcontroller, that also operates during load dump and thermal shutdown.
2. A power switch with protections, operated by an enable input.
3. Reset and hold outputs can be used to interface by the microcontroller. The reset signal can be used to call up the microcontroller and the hold output indicates regulator 1 voltage available and within range.
4. A supply pin which can withstand load dump pulses and negative supply voltage.
5. Regulator 2 will be switched on at a supply voltage >6.5 V and off at a voltage of regulator 2 <1.9 V.
6. Also there is a provision for use of a reserve supply capacitor that will hold enough energy for regulator 2 (5 V continuous) to allow a microcontroller to prepare for loss of voltage.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA3605Q	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage					
	operating		11	14.4	18	V
	reverse battery		−18	–	–	V
	regulator 2 on		2.4	14.4	18	V
	jump start	$t \leq 10$ minutes	–	–	30	V
	load dump protection	during ≤50 ms; $t_r \geq 2.5$ ms	–	–	50	V
$I_{q(tot)}$	total quiescent supply current	standby mode	–	500	600	µA
T_j	junction temperature		–	–	150	°C
Voltage regulators						
V_{REG1}	output voltage regulator 1	$0.5\ mA \leq I_{REG1} \leq 600\ mA$	9.5	10.0	10.5	V
V_{REG2}	output voltage regulator 2	$0.5\ mA \leq I_{REG2} \leq 300\ mA$; $V_P = 14.4\ V$	4.75	5.0	5.25	V
V_{REG3}	output voltage regulator 3	$0.5\ mA \leq I_{REG3} \leq 400\ mA$	4.75	5.0	5.25	V
Power switch						
$V_{sw(d)}$	drop-out voltage	$I_{sw} = 1\ A$	–	0.45	0.7	V
		$I_{sw} = 1.8\ A$	–	1	1.8	V
I_{swM}	peak current		3	–	–	A

BLOCK DIAGRAM

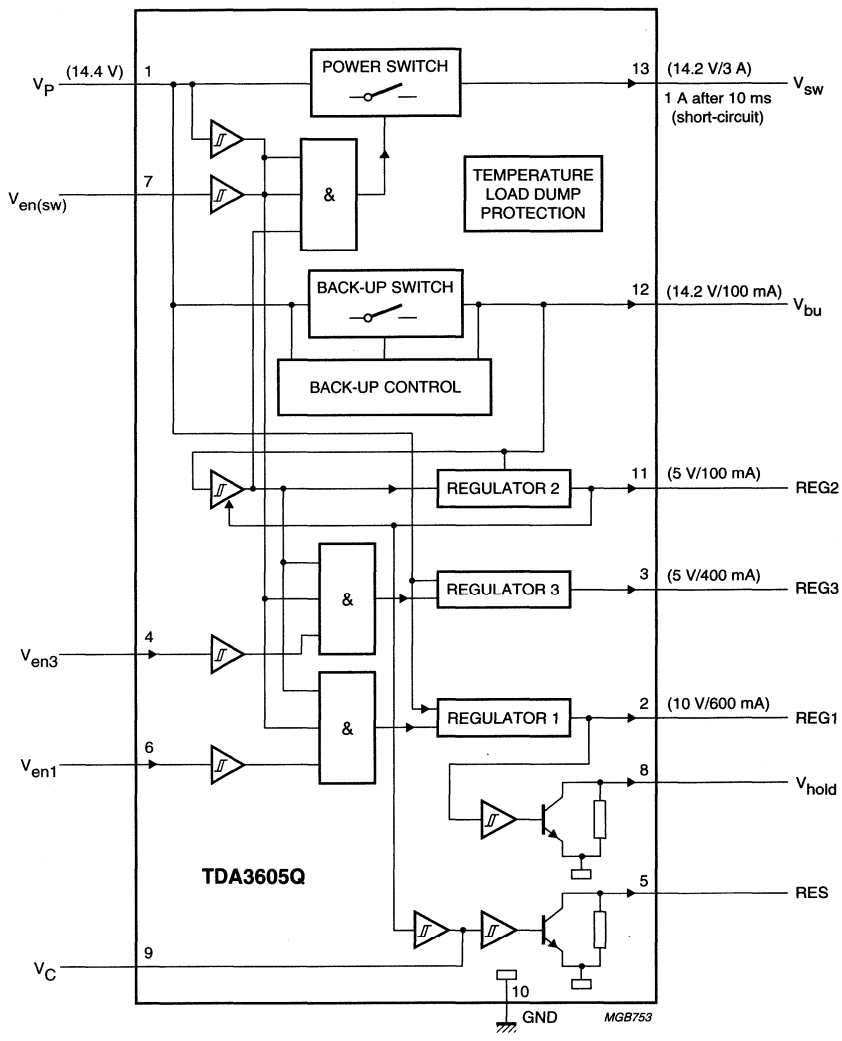


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	supply voltage
REG1	2	regulator 1 output
REG3	3	regulator 3 output
V_{en3}	4	enable input regulator 3
RES	5	reset output voltage
V_{en1}	6	enable input regulator 1
$V_{en(sw)}$	7	enable input power switch
V_{hold}	8	hold output
V_C	9	reset delay capacitor
GND	10	ground (0 V)
REG2	11	regulator 2 output
V_{bu}	12	back-up
V_{sw}	13	power switch output voltage

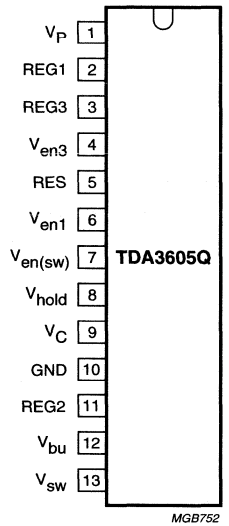


Fig.2 Pin configuration.

Multiple voltage regulator with switch and ignition buffers

TDA3609JR

FEATURES

General

- Extreme low noise behaviour and good stability with very small output capacitors
- Two V_P-state controlled regulators (regulator 1 and regulator 3) and a power switch
- Regulator 2, reset and ignition buffer operate during load dump and thermal shutdown
- Separate control pins for switching regulator 1, regulator 3 and the power switch
- Supply voltage range of −18 to +50 V
- Low reverse current of regulator 2
- Low quiescent current (when regulator 1, regulator 3, and power switch are switched-off)
- Hold output (only valid when regulator 1 is switched-on)
- Reset and hold outputs (open collector outputs)
- Adjustable reset delay time
- High ripple rejection
- Back-up capacitor for regulator 2
- Two independent ignition buffers (one inverted and with open collector output).

Protections

- Reverse polarity safe (down to −18 V without high reverse current)
- Able to withstand voltages up to 18 V at the outputs (supply line may be short-circuited)
- ESD protected on all pins
- Thermal protections with hysteresis
- Load dump protection
- Foldback current limit protection for regulators 1, 2 and 3
- Delayed second current limit protection for the power switch (at short-circuit)
- The regulator outputs and the power switch are DC short-circuited safe to ground and V_P.

GENERAL DESCRIPTION

The TDA3609JR is a multiple output voltage regulator with a power switch and ignition buffers, intended for use in car radios with or without a microcontroller. It contains:

- Two fixed voltage regulators with a foldback current protection (regulator 1 and regulator 3) and one fixed voltage regulator (regulator 2), intended to supply a microcontroller, that also operates during load dump and thermal shutdown
- A power switch with protections, operated by an enable input
- Reset and hold outputs that can be used to interface by the microcontroller. The reset-signal can be used to call up the microcontroller and the hold output indicates regulator 1 voltage available and within range.
- A supply pin which can withstand load dump pulses and negative supply voltages.
- Regulator 2 that will be switched on at a back-up voltage greater than 6.5 V and off when the output voltage of regulator 2 drops below 1.9 V.
- A provision for use of a reserve supply capacitor that will hold enough energy for regulator 2 (5 V continuous) to allow a microcontroller to prepare for loss of voltage.
- An inverted ignition 1 input with open collector output stage.
- An ignition 2 input Schmitt trigger with push pull output stage.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA3609JR	DBS17P	plastic DIL-bent-SIL (special bent) power package; 17 leads (lead length 12 mm)	SOT475-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage					
	operating		11	14.4	18	V
	reverse polarity	non-operating	–	–	−18	V
	regulator 2 on		2.4	14.4	50	V
	jump start	$t \leq 10$ minutes	–	–	30	V
	load dump protection	$t \leq 50$ ms; $t_r \geq 2.5$ ms	–	–	50	V
$I_{q(tot)}$	total quiescent supply current	standby mode	–	500	600	µA
T_j	junction temperature		–	–	150	°C
Voltage regulators						
$V_{O(REG1)}$	output voltage regulator 1	$1\ mA \leq I_{REG1} \leq 600\ mA$	9.5	10.0	10.5	V
$V_{O(REG2)}$	output voltage regulator 2	$0.5\ mA \leq I_{REG2} \leq 150\ mA$; $V_P = 14.4$ V	4.75	5.0	5.25	V
$V_{O(REG3)}$	output voltage regulator 3	$1\ mA \leq I_{REG3} \leq 500\ mA$	4.75	5.0	5.25	V
Power switch						
V_d	drop-out voltage	$I_{sw} = 1$ A	–	0.45	0.7	V
		$I_{sw} = 1.8$ A	–	1	1.8	V
I_M	peak current		3	–	–	A

BLOCK DIAGRAM

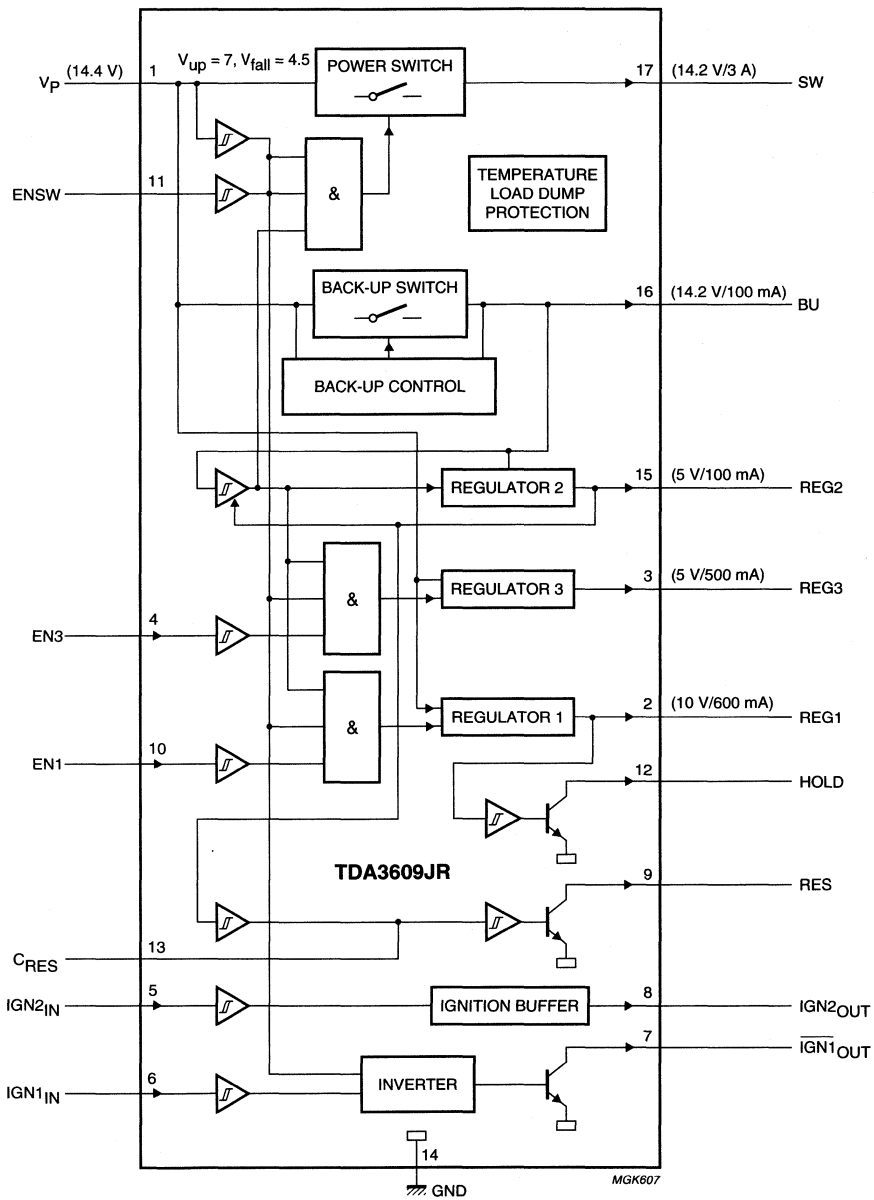


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	supply voltage
REG1	2	regulator 1 output
REG3	3	regulator 3 output
EN3	4	enable input regulator 3
$IGN2_{IN}$	5	ignition 2 input
$IGN1_{IN}$	6	ignition 1 input
$\overline{IGN1}_{OUT}$	7	ignition 1 output (active LOW)
$IGN2_{OUT}$	8	ignition 2 output
RES	9	reset output
EN1	10	enable input regulator 1
ENSW	11	enable input power switch
HOLD	12	hold output
C_{RES}	13	reset delay capacitor
GND	14	ground
REG2	15	regulator 2 output
BU	16	back-up
SW	17	power switch output

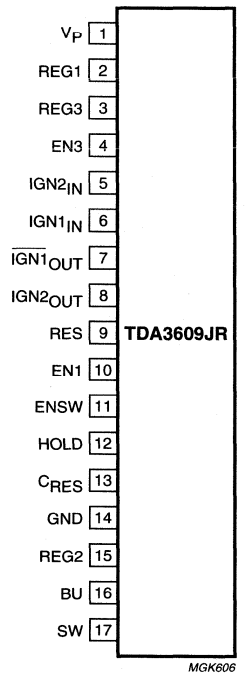


Fig.2 Pin configuration.

1 W BTL audio amplifier TDA8541

FEATURES

- Flexibility in use
- Few external components
- Low saturation voltage of output stage
- Gain can be fixed with external resistors
- Standby mode controlled by CMOS compatible levels
- Low standby current
- No switch-on/switch-off plops
- High supply voltage ripple rejection
- Protected against electrostatic discharge
- Outputs short-circuit safe to ground, V_{CC} and across the load
- Thermally protected.

GENERAL DESCRIPTION

The TDA8541(T) is a one channel audio power amplifier for an output power of 1 W with an 8 Ω load at a 5 V supply. The circuit contains a BTL amplifier with a complementary PNP-NPN output stage and standby/mute logic. The TDA8541T comes in an 8 pin SO package and the TDA8541 in an 8 pin DIP package.

APPLICATIONS

- Portable consumer products
- Personal computers
- Telephony.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		2.2	5	18	V
I_q	quiescent current	V_{CC} = 5 V	–	8	12	mA
I_{stb}	standby current		–	–	10	μA
P_o	output power	THD = 10%; R_L = 8 Ω; V_{CC} = 5 V	1	–	–	W
THD	total harmonic distortion	P_o = 0.5 W	–	0.15	–	%
SVRR	supply voltage ripple rejection		50	–	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8541T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
TDA8541	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1

BLOCK DIAGRAM

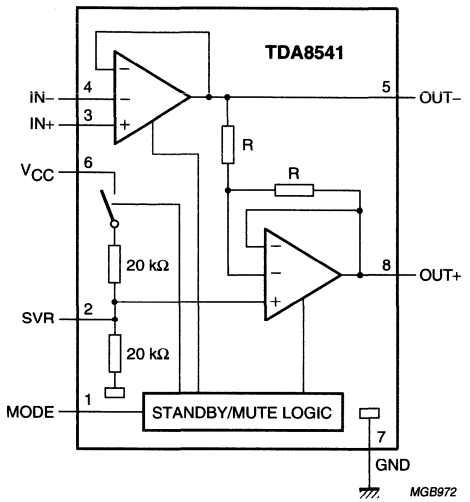


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
MODE	1	operating mode select (standby, mute, operating)
SVR	2	half supply voltage, decoupling ripple rejection
IN+	3	positive input
IN−	4	negative input
OUT−	5	negative loudspeaker terminal
V_{CC}	6	supply voltage
GND	7	ground
OUT+	8	positive loudspeaker terminal

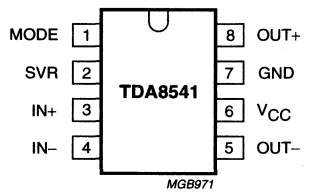


Fig.2 Pin configuration.

2 × 1 W BTL audio amplifier TDA8542

FEATURES

- Flexibility in use
- Few external components
- Low saturation voltage of output stage
- Gain can be fixed with external resistors
- Standby mode controlled by CMOS compatible levels
- Low standby current
- No switch-on/switch-off plops
- High supply voltage ripple rejection
- Protected against electrostatic discharge
- Outputs short-circuit safe to ground, V_{CC} and across the load
- Thermally protected.

GENERAL DESCRIPTION

The TDA8542(T) is a two channel audio power amplifier for an output power of 2 × 1 W with an 8 Ω load at a 5 V supply. The circuit contains two BTL amplifiers with a complementary PNP-NPN output stage and standby/mute logic. The TDA8542T comes in a 16 pin SO package and the TDA8542 in a 16 pin DIP package.

APPLICATIONS

- Portable consumer products
- Personal computers
- Motor-driver (servo).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		2.2	5	18	V
I_q	quiescent current	V_{CC} = 5 V	–	15	22	mA
I_{stb}	standby current		–	–	10	μA
P_o	output power	THD = 10%; R_L = 8 Ω; V_{CC} = 5 V	1	–	–	W
THD	total harmonic distortion	P_o = 0.5 W	–	0.15	–	%
SVRR	supply voltage ripple rejection		50	–	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8542T	SO16L	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
TDA8541	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1

BLOCK DIAGRAM

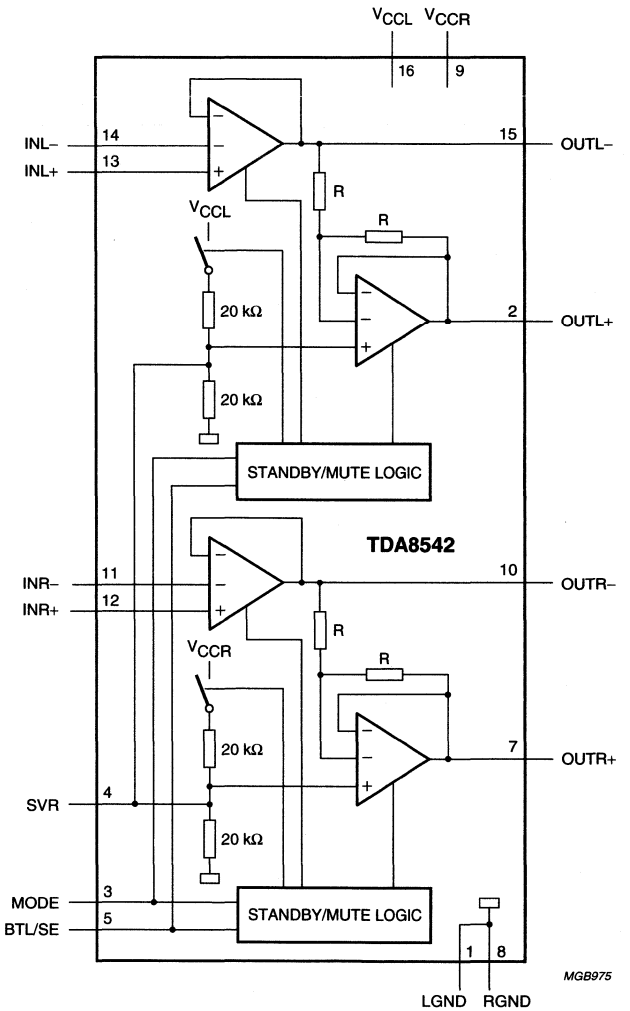


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LGND	1	ground, left channel
OUTL+	2	positive loudspeaker terminal, left channel
MODE	3	operating mode select (standby, mute, operating)
SVR	4	half supply voltage, decoupling ripple rejection
BTL/SE	5	BTL loudspeaker or SE headphone operation
n.c.	6	not connected
OUTR+	7	positive loudspeaker terminal, right channel
RGND	8	ground, right channel
V_{CCR}	9	supply voltage, right channel
OUTR–	10	negative loudspeaker terminal, right channel
INR–	11	negative input, right channel
INR+	12	positive input, right channel
INL+	13	positive input, left channel
INL–	14	negative input, left channel
OUTL–	15	negative loudspeaker terminal, left channel
V_{CCL}	16	supply voltage, left channel

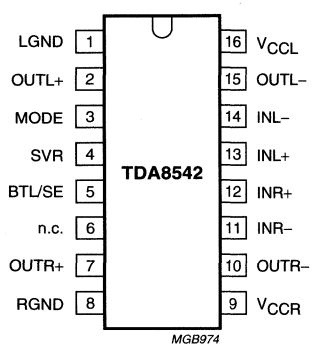


Fig.2 Pin configuration.

Low-voltage stereo headphone amplifier TDA8559

FEATURES

- Operating voltage from 1.9 to 30 V
- Very low quiescent current
- Low distortion
- Few external components
- Differential inputs
- Usable as a mono amplifier in Bridge-Tied Load (BTL) or stereo Single-Ended (SE)
- Single-ended mode without loudspeaker capacitor
- Mute and standby mode
- Short-circuit proof to ground, to supply voltage (<10 V) and across load
- No switch on or switch off clicks
- ESD protected on all pins.

APPLICATIONS

- Portable telephones
- Walk-mans
- Portable audio
- Mains fed equipment.

GENERAL DESCRIPTION

The TDA8559 is a stereo amplifier that operates over a wide supply voltage range from 1.9 to 30 V and consumes a very low quiescent current. This makes it suitable for battery fed applications (2 × 1.5 V cells). Because of an internal voltage buffer, this device can be used with or without a capacitor connected in series with the load. It can be applied as a headphone amplifier, but also as a mono amplifier with a small speaker (25 Ω), or as a line driver in mains applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_P	operating supply voltage		1.9	3	30	V
$I_{q(tot)}$	total quiescent current		–	2.75	4	mA
I_{stb}	standby supply current		–	–	10	μA
Stereo application						
P_o	output power	THD = 10%	30	35	–	mW
THD	total harmonic distortion	P_o = 20 mW; f_i = 1 kHz	–	0.075	0.15	%
		P_o = 20 mW; f_i = 10 kHz	–	0.1	–	%
G_v	voltage gain		25	26	27	dB
f_{ss}	small signal roll-off frequency	–1 dB	–	750	–	kHz
BTL application						
P_o	output power	THD = 10%	125	140	–	mW
THD	total harmonic distortion	P_o = 70 mW; f_i = 1 kHz	–	0.05	0.1	%
		P_o = 70 mW; f_i = 10 kHz	–	0.2	–	%
G_v	voltage gain		31	32	33	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8559	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
TDA8559T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM

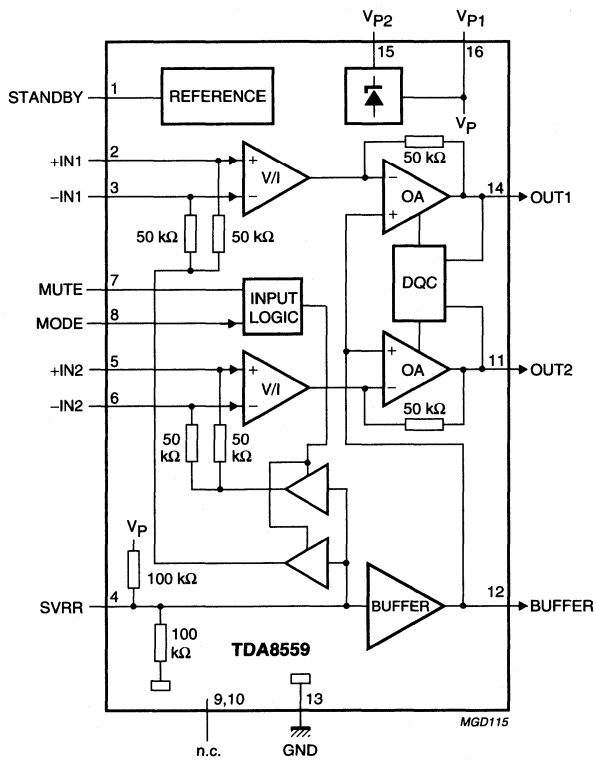


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
STANDBY	1	standby select
+IN1	2	non-inverting input 1
–IN1	3	inverting input 1
SVRR	4	supply voltage ripple rejection
+IN2	5	non-inverting input 2
–IN2	6	inverting input 2
MUTE	7	mute select
MODE	8	input mode select
n.c.	9	not connected
n.c.	10	not connected
OUT2	11	output 2
BUFFER	12	buffer output ($0.5V_P$)
GND	13	ground
OUT1	14	output 1
V_{P2}	15	high supply voltage
V_{P1}	16	low supply voltage

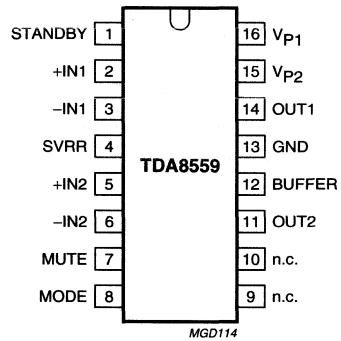


Fig.2 Pin configuration.

2 × 40 W/2 Ω stereo BTL car radio power amplifier with diagnostic facility

TDA8560Q

FEATURES

- Requires very few external components
- High output power
- 4 Ω and 2 Ω load impedance
- Low output offset voltage
- Fixed gain
- Diagnostic facility (distortion, short-circuit and temperature detection)
- Good ripple rejection
- Mode select switch (operating, mute and standby)
- Load dump protection
- Short-circuit safe to ground, to V_P and across the load
- Low power dissipation in any short-circuit condition
- Thermally protected
- Reverse polarity safe
- Electrostatic discharge protection
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance.

GENERAL DESCRIPTION

The TDA8560Q is an integrated class-B output amplifier in a 13-lead single-in-line (SIL) power package.
It contains 2 × 40 W/2 Ω amplifiers in BTL configuration.

The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	operating supply voltage		6.0	14.4	18	V
I_{ORM}	repetitive peak output current		–	–	7.5	A
$I_{q(tot)}$	total quiescent current		–	115	–	mA
I_{sb}	standby current		–	0.1	100	μA
I_{sw}	switch-on current		–	–	40	μA
$\|Z_I\|$	input impedance		25	30	–	kΩ
P_o	output power	R_L = 4 Ω; THD = 10%	–	25	–	W
		R_L = 2 Ω; THD = 10%	–	40	–	W
SVRR	supply voltage ripple rejection	R_s = 0 Ω	–	45	–	dB
α_{cs}	channel separation	R_s = 10 kΩ	–	50	–	dB
G_v	closed loop voltage gain		39	40	41	dB
V_{no}	noise output voltage	R_s = 0 Ω	–	–	250	μV
$\|\Delta V_O\|$	DC output offset voltage		–	–	200	mV

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8560Q	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6

BLOCK DIAGRAM

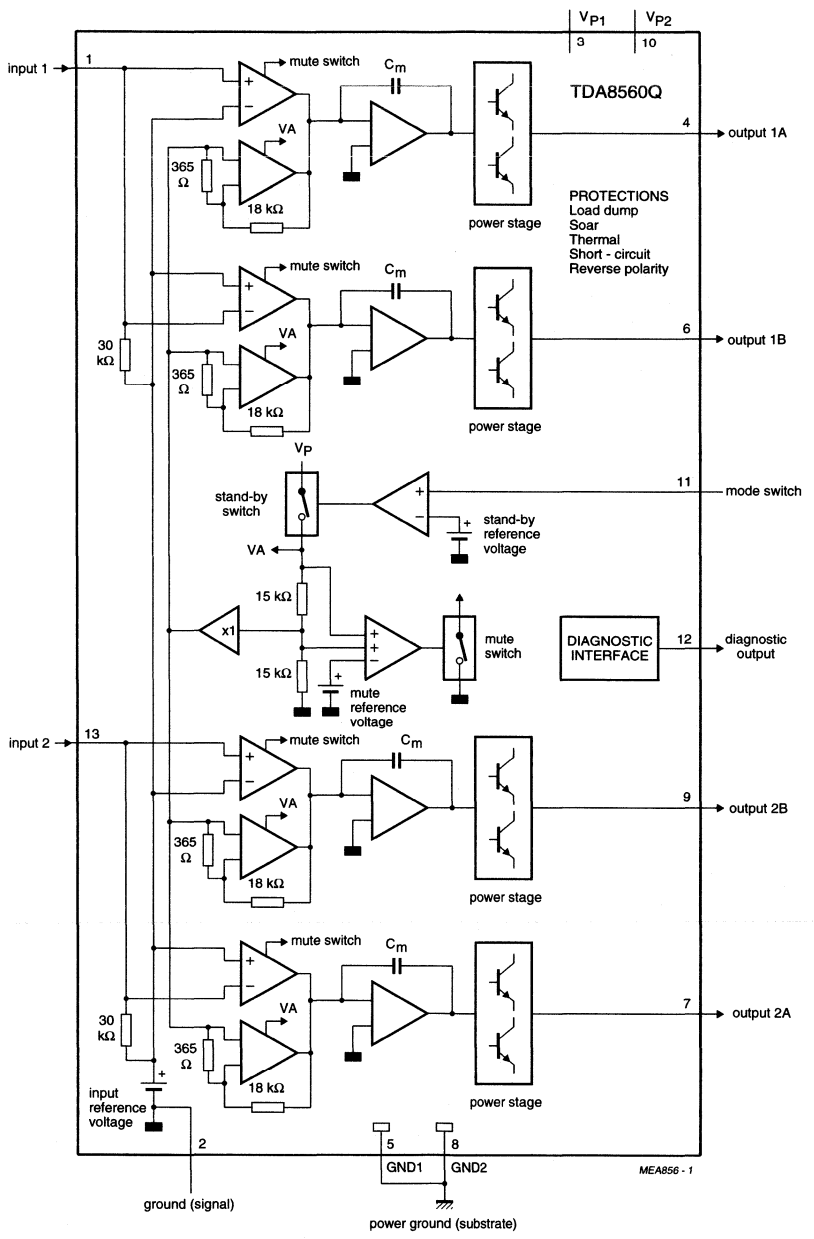


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
IN 1	1	input 1
GND(S)	2	signal ground
V_{P1}	3	supply voltage 1
OUT 1A	4	output 1A
GND1	5	power ground 1
OUT 1B	6	output 1B
OUT 2A	7	output 2A
GND2	8	power ground 2
OUT 2B	9	output 2B
V_{P2}	10	supply voltage 2
MODE	11	mode switch input
V_{DIAG}	12	diagnostic output
IN 2	13	input 2

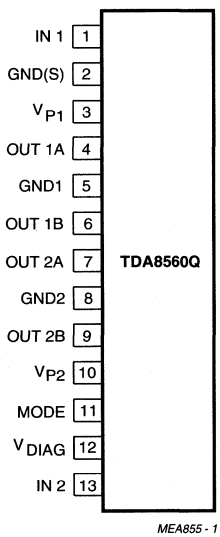


Fig.2 Pin configuration.

2 x 24 W BTL or 4 x 12 W single-ended car radio power amplifier

TDA8561Q

FEATURES

- Requires very few external components
- High output power
- Flexibility in use - Quad single-ended or stereo BTL
- Low output offset voltage
- Fixed gain
- Diagnostic facility (distortion, short-circuit and temperature detection)
- Good ripple rejection
- Mode select switch (operating, mute and stand-by)
- Load dump protection
- AC and DC short-circuit safe to ground and to V_P
- Low power dissipation in any short-circuit condition
- Thermally protected
- Reverse polarity safe
- Electrostatic discharge protection
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance
- Identical inputs (inverting and non-inverting).

GENERAL DESCRIPTION

The TDA8561Q is an integrated class-B output amplifier in a 17-lead single-in-line (SIL) power package. It contains 4 x 12 W single-ended or 2 x 24 W bridge amplifiers.

The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive operating supply voltage		6	14.4	18	V
I_{ORM}	repetitive peak output current		–	–	4	A
I_P	total quiescent current		–	80	–	mA
I_{sb}	stand-by current		–	0.1	100	μA
Stereo BTL application						
P_O	output power	4 Ω; THD = 10%	–	24	–	W
RR	supply voltage ripple rejection		48	–	–	dB
V_{no}	noise output voltage	R_s = 0 Ω	–	70	–	μV
$\|Z_I\|$	input impedance		25	–	–	kΩ
$\|\Delta V_O\|$	DC output offset voltage		–	–	150	mV
Quad single-ended application						
P_O	output power	THD = 10%				
		4 Ω	–	7	–	W
		2 Ω	–	12	–	W
RR	supply voltage ripple rejection		48	–	–	dB
V_{no}	noise output voltage	R_s = 0 Ω	–	50	–	μV
$\|Z_I\|$	input impedance		50	–	–	kΩ

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8561Q	17	DBS	plastic	SOT243R[1]

Note

1. SOT243-1; 1996 August 30.

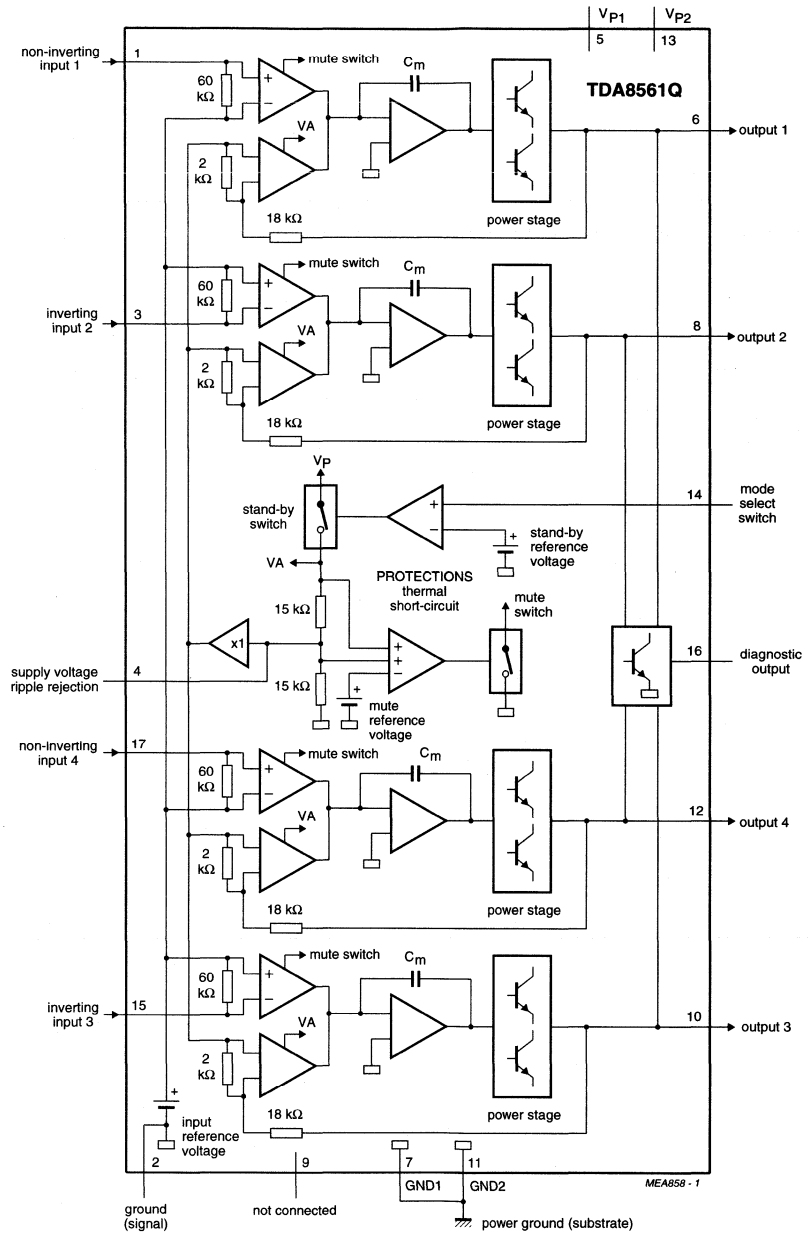


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
–INV 1	1	non-inverting input 1
GND(S)	2	signal ground
INV 2	3	inverting input 2
RR	4	supply voltage ripple rejection
V_{P1}	5	supply voltage
OUT 1	6	output 1
GND1	7	power ground 1
OUT 2	8	output 2
n.c.	9	not connected
OUT 3	10	output 3
GND2	11	power ground 2
OUT 4	12	output 4
V_{P2}	13	supply voltage
MODE	14	mode select switch input
INV 3	15	inverting input 3
V_{DIAG}	16	diagnostic output
–INV 4	17	non-inverting input 4

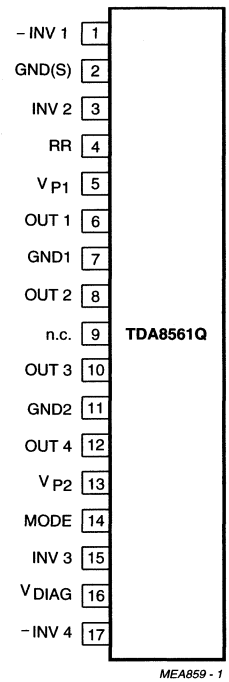


Fig.2 Pin configuration.

2 × 40 W/2 Ω stereo BTL car radio power amplifier with diagnostic facility

TDA8563Q

FEATURES

- Requires very few external components
- High output power
- 4 Ω and 2 Ω load impedance
- Low output offset voltage
- Fixed gain
- Diagnostic facility (distortion, short-circuit and temperature detection)
- Good ripple rejection
- Mode select switch (operating, mute and standby)
- Load dump protection
- Short-circuit safe to ground, to V_P and across the load
- Low power dissipation in any short-circuit condition
- Thermally protected
- Reverse polarity safe
- Electrostatic discharge protection
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance.

GENERAL DESCRIPTION

The TDA8563Q is an integrated class-B output amplifier in a 13-lead single-in-line (SIL) power package.
It contains 2 × 40 W/2 Ω amplifiers in BTL configuration.

The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	operating supply voltage		6.0	14.4	18	V
I_{ORM}	repetitive peak output current		–	–	7.5	A
$I_{q(tot)}$	total quiescent current		–	115	–	mA
I_{sb}	standby current		–	0.1	100	μA
I_{sw}	switch-on current		–	–	40	μA
$\lvert Z_I \rvert$	input impedance		25	30	–	kΩ
P_o	output power	R_L = 4 Ω; THD = 10%	–	25	–	W
		R_L = 2 Ω; THD = 10%	–	40	–	W
SVRR	supply voltage ripple rejection	R_s = 0 Ω	–	60	–	dB
α_{cs}	channel separation	R_s = 10 kΩ	–	50	–	dB
G_v	closed loop voltage gain		25	26	27	dB
V_{no}	noise output voltage	R_s = 0 Ω	–	–	120	μV
$\lvert \Delta V_O \rvert$	DC output offset voltage		–	–	150	mV

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8563Q	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6

BLOCK DIAGRAM

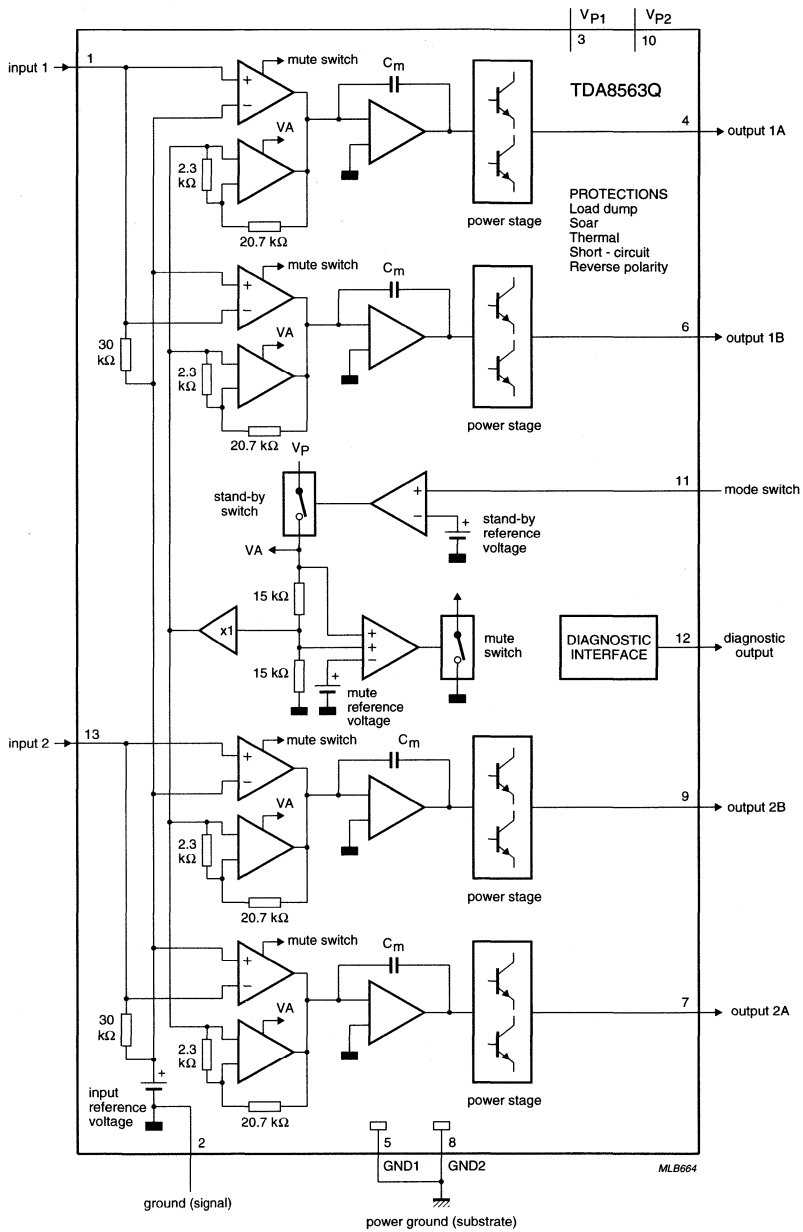


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
IN 1	1	input 1
GND(S)	2	signal ground
V_{P1}	3	supply voltage 1
OUT 1A	4	output 1A
GND1	5	power ground 1
OUT 1B	6	output 1B
OUT 2A	7	output 2A
GND2	8	power ground 2
OUT 2B	9	output 2B
V_{P2}	10	supply voltage 2
MODE	11	mode switch input
V_{DIAG}	12	diagnostic output
IN 2	13	input 2

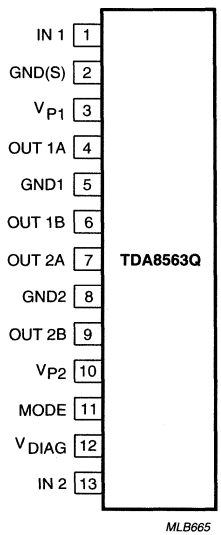


Fig.2 Pin configuration.

4 × 25 W BTL quad car radio power amplifier

TDA8567Q

FEATURES

- Requires very few external components
- High output power
- Low output offset voltage
- Fixed gain
- Diagnostic facility (distortion, short-circuit and temperature pre-warning)
- Good ripple rejection
- Mode select switch (operating, mute and standby)
- Load dump protection
- Short-circuit safe to ground and to V_P and across the load
- Low power dissipation in any short-circuit condition
- Thermally protected
- Reverse polarity safe
- Electrostatic discharge protection
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance
- Pin compatible with the TDA8568Q, except for the gain.

GENERAL DESCRIPTION

The TDA8567Q is an integrated class-B output amplifier in a 23-lead Single-In-Line (SIL) plastic power package. It contains four amplifiers in BTL configuration, each with a gain of 26 dB. The output power is 4 × 25 W in a 4 Ω load.

APPLICATIONS

- The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	operating supply voltage		6	14.4	18	V
I_{ORM}	repetitive peak output current		–	–	7.5	A
$I_{q(tot)}$	total quiescent current		–	230	–	mA
I_{stb}	standby current		–	0.2	100	μA
I_{sw}	switch-on current		–	–	80	μA
$\lvert Z_i \rvert$	input impedance		25	30	–	kΩ
P_o	output power	THD = 10%	–	25	–	W
SVRR	supply voltage ripple rejection	R_s = 0 Ω	–	60	–	dB
α_{cs}	channel separation	R_s = 10 kΩ	–	50	–	dB
G_v	closed loop voltage gain		25	26	27	dB
$V_{n(o)}$	noise output voltage	R_s = 0 Ω	–	–	120	μV
$\lvert \Delta V_O \rvert$	DC output offset voltage		–	–	150	mV

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8567Q	DBS23P	plastic DIL-bent-SIL power package; 23 leads (straight lead length 3.2 mm)	SOT411-1

BLOCK DIAGRAM

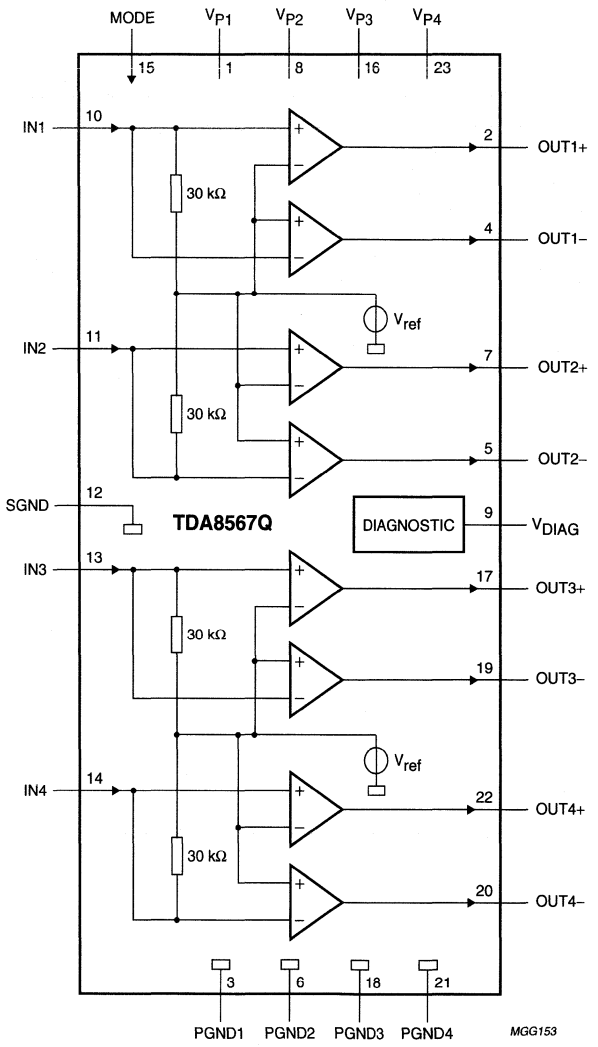


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{P1}	1	supply voltage 1
OUT1+	2	output 1+
PGND1	3	power ground 1
OUT1–	4	output 1–
OUT2–	5	output 2–
PGND2	6	power ground 2
OUT2+	7	output 2+
V_{P2}	8	supply voltage 2
V_{DIAG}	9	diagnostic output
IN1	10	input 1
IN2	11	input 2
SGND	12	signal ground
IN3	13	input 3
IN4	14	input 4
MODE	15	mode select switch input
V_{P3}	16	supply voltage 3
OUT3+	17	output 3+
PGND3	18	power ground 3
OUT3–	19	output 3–
OUT4–	20	output 4–
PGND4	21	power ground 4
OUT4+	22	output 4+
V_{P4}	23	supply voltage 4

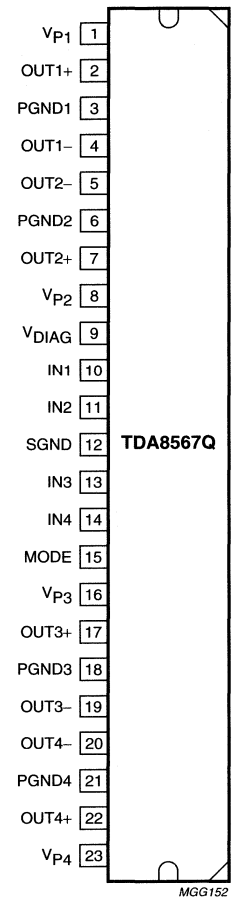


Fig.2 Pin configuration.

Dual common-mode rejection differential line receiver

TDA8579

FEATURES

- Excellent common-mode rejection, up to high frequencies
- Elimination of source resistance dependency in the common-mode rejection
- Few external components
- High supply voltage ripple rejection
- Low noise
- Low distortion
- All pins protected against electrostatic discharge
- AC and DC short-circuit safe to ground and V_{CC}
- Fast DC settling.

GENERAL DESCRIPTION

The TDA8579 is a two channel differential amplifier with 0 dB gain and low distortion. The device has been primarily developed for car radio applications where long connections between signal sources and amplifiers (or boosters) are necessary and where ground noise has to be eliminated. The device is intended to be used to receive line inputs in audio applications that require a high level of common-mode rejection. The device is contained in an 8-pin small outline (SO) or dual in-line (DIP) package.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		5.0	8.5	18	V
I_{CC}	supply current	V_{CC} = 8.5 V	–	11	14	mA
G_v	voltage gain		−0.5	0	+0.5	dB
SVRR	supply voltage ripple rejection		55	60	–	dB
V_{no}	noise output voltage		–	3.7	5.0	μV
$\lvert Z_i \rvert$	input impedance		100	240	–	kΩ
CMRR	common-mode rejection ratio	R_s = 0 Ω	–	80	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8579	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
TDA8579T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

Dual common-mode rejection differential line receiver

TDA8579

BLOCK DIAGRAM

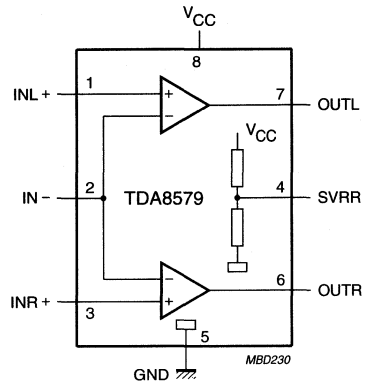


Fig.1 Block diagram.

FUNCTIONAL DESCRIPTION

The TDA8579 contains two identical differential amplifiers with a voltage gain of 0 dB. The device is intended to receive line input signals for audio applications. The TDA8579 has a very high level of common-mode rejection and thus eliminates ground noise. The common-mode rejection remains constant up to high frequencies (the amplifier gain is fixed at 0 dB). The inputs have a high input impedance. The output stage is a class AB stage with a low output impedance. For a large common-mode rejection, also at low frequencies, an electrolytic capacitor connected to the negative input is advised. Because the input impedance is relatively high, this results in a large settling time of the DC input voltage. Therefore a quick-charge circuit is included to charge the input capacitor within 0.2 seconds.

All input and output pins are protected against high electrostatic discharge conditions (4000 V, 150 pF, 150 Ω).

PINNING

SYMBOL	PIN	DESCRIPTION
INL+	1	positive input left
IN−	2	common negative input
INR+	3	positive input right
SVRR	4	half supply voltage
GND	5	ground
OUTR	6	output right
OUTL	7	output left
V_{CC}	8	supply voltage

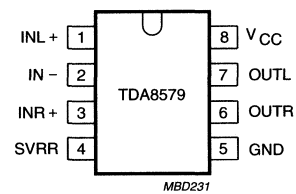


Fig.2 Pin configuration.

Dual Dolby* B-type noise reduction circuit for playback applications

TEA0675

FEATURES

- Dual noise reduction (NR) channels
- Head pre-amplifiers
- Reverse head switching
- Automatic Music Search (AMS)
- Music scan
- Equalization with electronically switched time constants
- Dolby reference level = 387.5 mV
- 24 pins
- Improved EMC behaviour.

GENERAL DESCRIPTION

The TEA0675 is a bipolar integrated circuit that provides two channels of Dolby B noise reduction for playback applications in car radios. It includes head and equalization amplifiers with electronically switchable time constants. Furthermore it includes electronically switchable inputs for tape drivers with reverse heads.

This device also detects pauses of music in the Automatic Music Search (AMS) scan mode, for applications with an intelligent controlled tape driver, or AMS-latch mode, for applications with a simple controlled tape driver. For both modes, the delay time can be fixed externally by a resistor. The device operates with power supplies in the range of 7.6 to 12 V, output overload level increasing with increase in supply voltage.

Current drain varies with the following variables:

supply voltage

noise reduction on/off

AMS on/off.

Because of this current drain variation it is advisable to use a regulated power supply or a supply with a long time constant.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	7.6	–	12	V
I_{CC}	supply current	–	26	31	mA
$\frac{S+N}{N}$	signal plus noise-to-noise ratio	78	84	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA0675	SDIP24	plastic shrink dual in-line package; 24 leads (400 mil)	SOT234-1
TEA0675T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

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BLOCK DIAGRAM

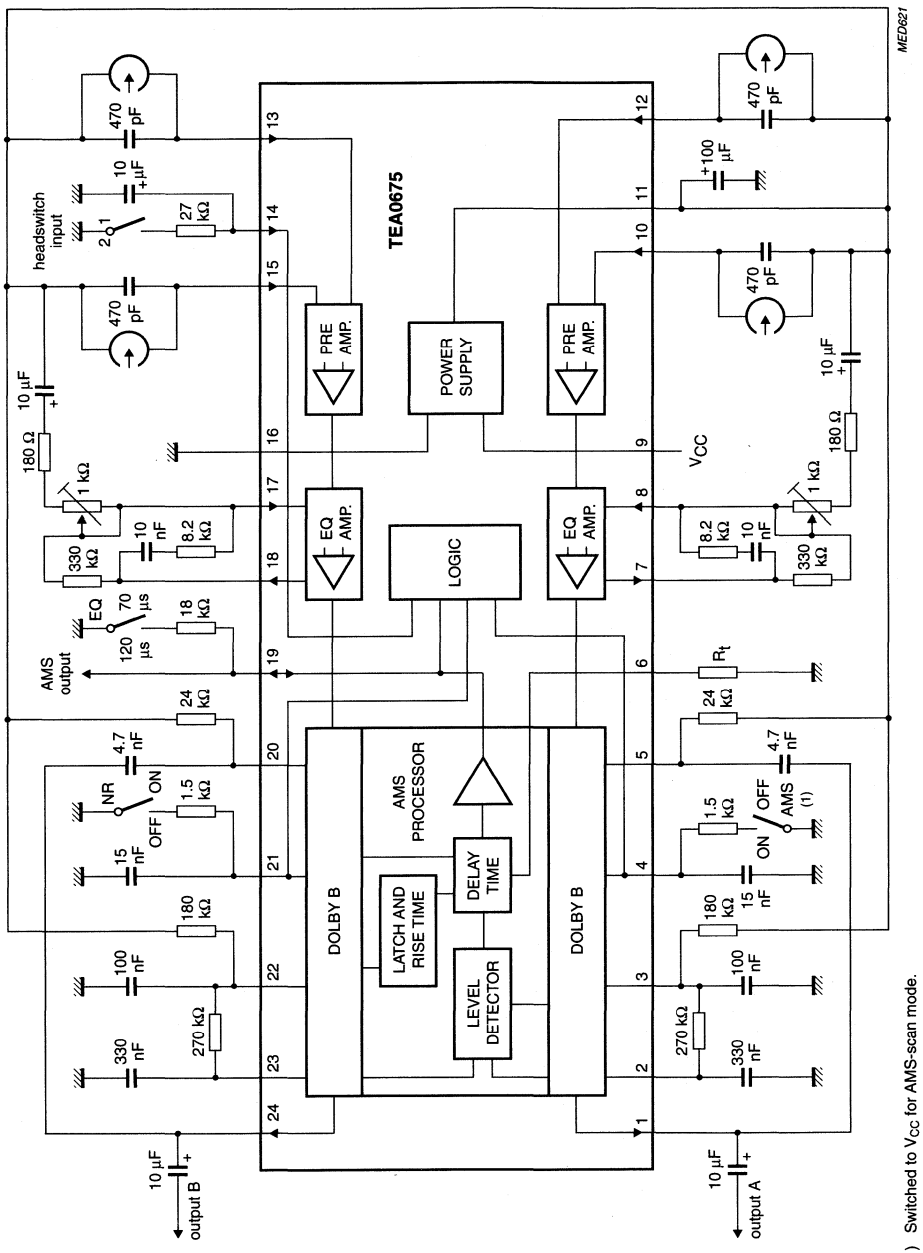

Fig.1 Block and application diagram.

(1) Switched to V_{CC} for AMS-scan mode.

PINNING

SYMBOL	PIN	DESCRIPTION
OUTA	1	output channel A
INTA	2	integrating filter channel A
CONTRA	3	control voltage channel A
HPA	4	high-pass filter channel A
SCA	5	side chain channel A
TD	6	delay time constant
EQA	7	equalizing output channel A
EQFA	8	equalizing input channel A
V_{CC}	9	supply voltage
INA1	10	input channel A1 (forward or reverse)
V_{ref}	11	reference voltage
INA2	12	input channel A2 (reverse or forward)
INB2	13	input channel B2 (reverse or forward)
HS	14	head switch input
INB1	15	input channel B1 (forward or reverse)
GND	16	ground
EQFB	17	equalizing input channel B
EQB	18	equalizing output channel B
AMSEQ	19	AMS output and EQ switch input
SCB	20	side chain channel B
HPB	21	high-pass filter channel B
CONTRB	22	control voltage channel B
INTB	23	integrating filter channel B
OUTB	24	output channel B

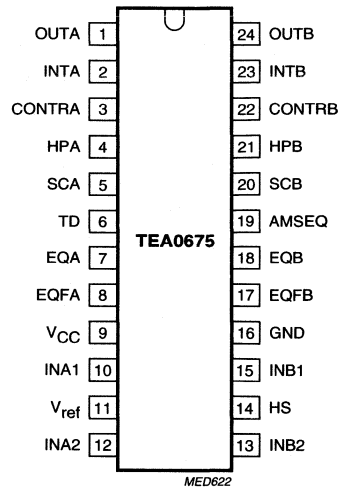

Fig.2 Pin configuration.

Dual pre-amplifier and equalizer for reverse tape decks

TEA0677T

FEATURES

- Head pre-amplifiers
- Reverse head switching
- Equalization with electronically switched time constants
- 0 dB = 387.5 mV
- Pin compatible to TEA0675 Dolby B, music search IC.

GENERAL DESCRIPTION

The TEA0677T is a monolithic bipolar integrated circuit intended for applications in car radios. It includes head and equalization amplifiers with electronically switchable time constants. Furthermore it includes electronically switchable inputs for tape drives with reverse heads. The device is intended to replace the regular TEA0675T in low-cost car radios using the same PCB. External components that are necessary for Dolby B and music search features can be omitted.

The device will operate with power supplies in the range of 7.6 V to 12.0 V, output overload level increasing with increase in supply voltage. Current drain varies with supply voltage, so it is advisable to use a regulated power supply or a supply with a long time constant.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	7.6	10	12	V
I_{CC}	supply current	–	23	26	mA
(S + N)/N	signal-plus-noise to noise ratio	68	74	–	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA0677T	24	SO	plastic	SOT137A(1)

Note

1. SOT137-1; 1996 August 27.

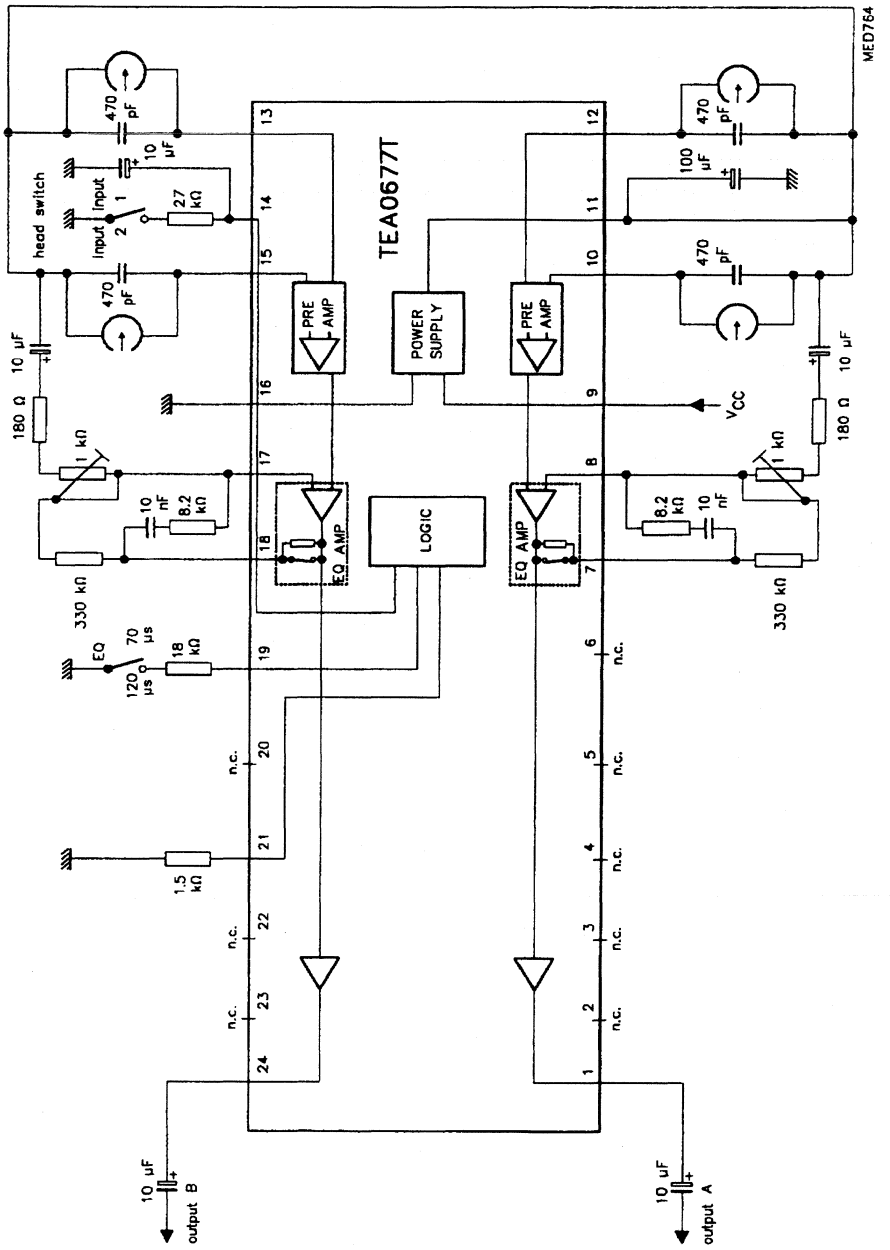

Fig.1 Block and application diagram.

Instead of potentiometers at EQ AMP fixed resistors may be used. The value depends on applied heads.

PINNING

SYMBOL	PIN	DESCRIPTION
OUTA	1	output channel A
n.c.	2	not connected
n.c.	3	not connected
n.c.	4	not connected
n.c.	5	not connected
n.c.	6	not connected
EQA	7	equalizing output channel A
EQFA	8	equalizing input channel A
V_{CC}	9	supply voltage
INA1	10	input channel A1 (forward or reverse)
V_{REF}	11	reference voltage
INA2	12	input channel A2 (reverse or forward)
INB2	13	input channel B2 (reverse or forward)
HS	14	head switch input
INB1	15	input channel B1 (forward or reverse)
GND	16	ground
EQFB	17	equalizing input channel B
EQB	18	equalizing output channel B
EQS	19	equalizing switch input
n.c.	20	not connected
ACUR	21	auxiliary current
n.c.	22	not connected
n.c.	23	not connected
OUTB	24	output channel B

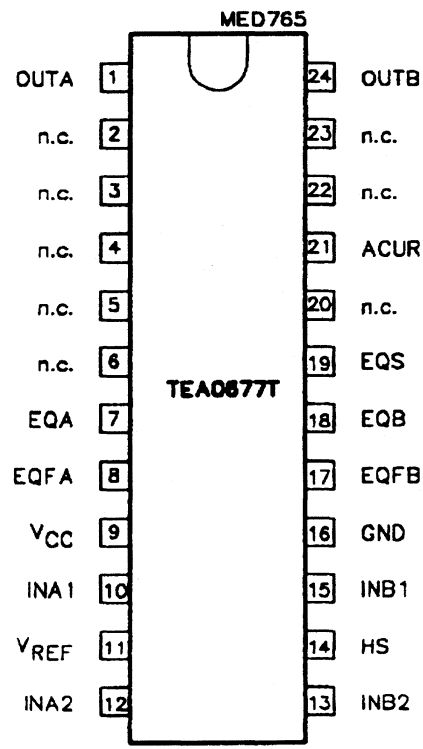

Fig.2 Pin configuration.

Dual Dolby* B-type noise reduction circuit, automatic music search, with differential outputs and mute

TEA0678

FEATURES

- Dual noise reduction (NR) channels
- Head pre-amplifiers
- Reverse head switching
- Automatic Music Search (AMS)
- Mute position
- Equalization with electronically switched time constants
- Dolby reference level = 387.5 mV
- 32 pins
- Switch inputs TTL compatible
- Differential output stage has:
  - Capability to drive 1.2 nF capacitive load
  - Capability to drive 1 kΩ load
  - Short-circuit proof
  - Short-circuit proof to 16 V via coupling capacitor.
- Improved EMC behaviour.

GENERAL DESCRIPTION

The TEA0678 is a bipolar integrated circuit that provides two channels of Dolby B noise reduction for playback applications in car radios. It includes head and equalization amplifiers with electronically switchable time constants. Furthermore it includes electronically switchable inputs for tape drivers with reverse heads. This device also detects pauses of music in Automatic Music Search (AMS) mode, with a delay time fixed externally by a resistor. The short-circuit proof output stage of the TEA0678 is differential and provides muting. The device will operate with power supplies in the range of 7.6 to 12 V, output overload level increasing with increase in supply voltage. Current drain varies with supply voltage, noise reduction on/off and AMS on/off so it is advisable to use a regulated power supply or a supply with a long time constant.

.Current drain varies with these variables:

Supply voltage

Noise reduction on/off

AMS on/off.

Because of this current drain variation it is advisable to use a regulated power supply or a supply with a long time constant.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	7.6	10	12	V
I_{CC}	supply current	–	25	28	mA
$\frac{S+N}{N}$	signal plus noise-to-noise ratio	78	84	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA0678	SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1
TEA0678T	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

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Dual Dolby* B-type noise reduction circuit, automatic music search, with differential outputs and mute

TEA0678

BLOCK DIAGRAM

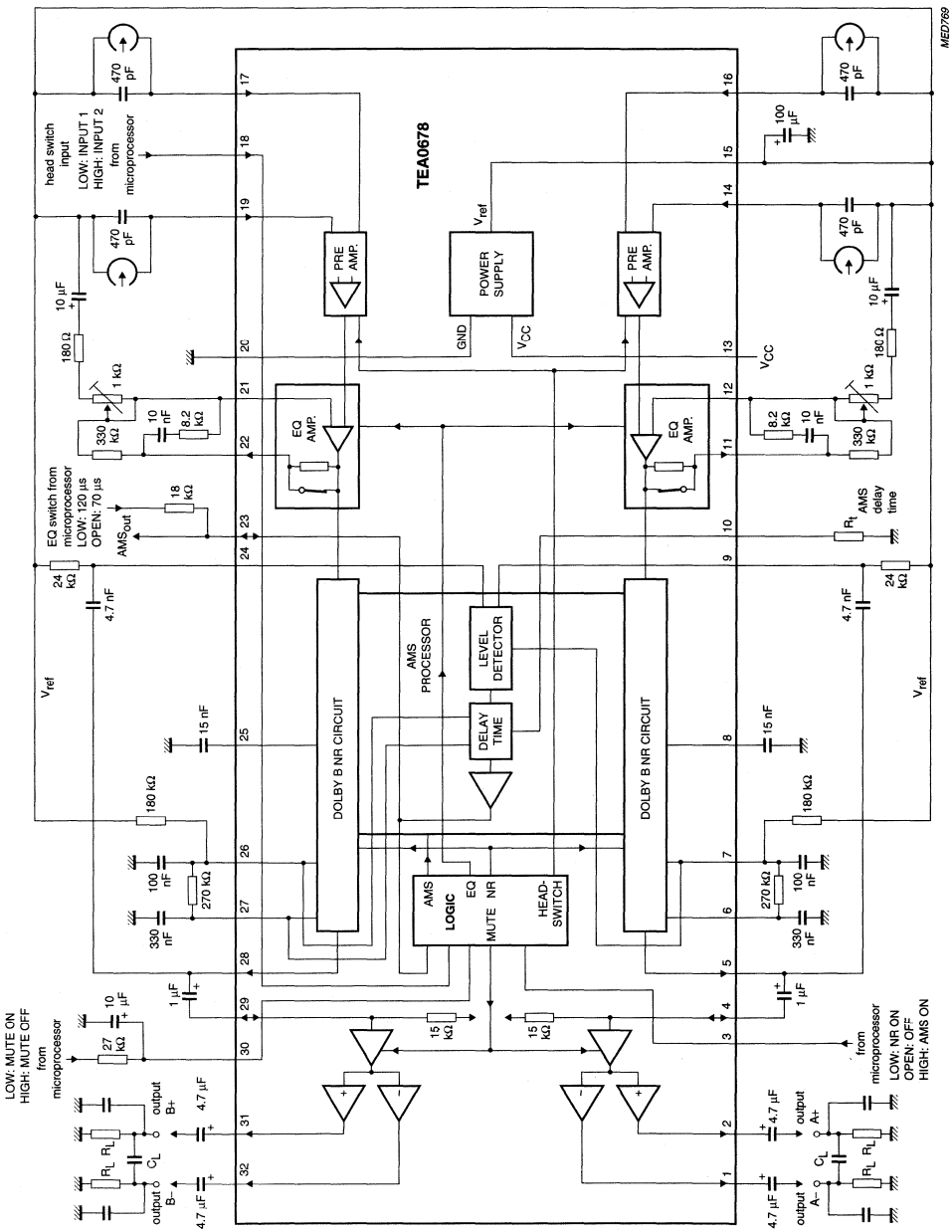


Fig.1 Block and application diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OUTA–	1	negative output channel A
OUTA+	2	positive output channel A
NR/AMS	3	noise reduction/music search switch
INCA	4	input mute/output stage channel A
OUTCA	5	output Dolby B processor channel A
INTA	6	integrating filter channel A
CONTRA	7	control voltage channel A
HPA	8	high-pass filter channel A
SCA	9	side chain channel A
TD	10	delay time constant
EQA	11	equalizing output channel A
EQFA	12	equalizing feedback channel A
V_{CC}	13	supply voltage
INA1	14	input channel A1 (forward or reverse)
V_{ref}	15	reference voltage
INA2	16	input channel A2 (reverse or forward)
INB2	17	input channel B2 (reverse or forward)
HS	18	head switch input
INB1	19	input channel B1 (forward or reverse)
GND	20	ground
EQFB	21	equalizing feedback channel B
EQB	22	equalizing output channel B
AMSEQ	23	AMS output and EQ switch input
SCB	24	side chain channel B
HPB	25	high-pass filter channel B
CONTRB	26	control voltage channel B
INTB	27	integrating filter channel B
OUTCB	28	output Dolby B processor channel B
INCB	29	input mute/output stage channel B
MUTE	30	mute switch
OUTB+	31	positive output channel B
OUTB–	32	negative output channel B

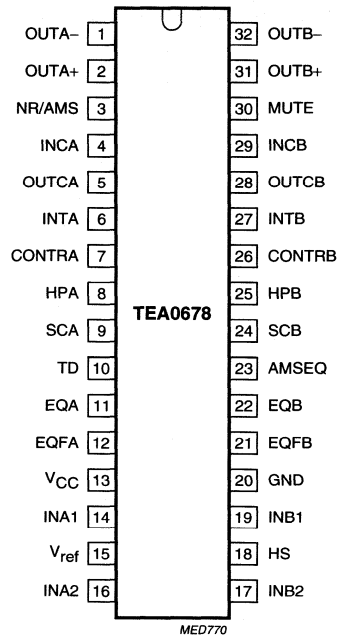


Fig.2 Pin configuration.

Self Tuned Radio (STR) TEA5757; TEA5759

FEATURES

- The tuning system has an optimized IC partitioning both from application (omitting interferences) and flexibility (removable front panel option) point of view: the tuning synthesizer is on-chip with the radio
- The tuning quality is superior and requires no IF-counter for stop-detection; it is insensitive to ceramic filter tolerances
- In combination with the microcontroller, fast, low-power operation of preset mode, manual-search, auto-search and auto-store are possible
- The local (internal) controller function facilitates reduced and simplified microcontroller software
- The high integration level (radio and tuning synthesizer on one chip) means fewer external components with regard to the communication between the radio and the microcontroller (90% less components compared to the digital tuning application of a radio IC with external PLL tuning function) and a simple and small PCB
- There will be no application considerations for the tuning system, with regards to quality and high integration level, since there will be no external 110 MHz buffers, loop filter or false lock elimination
- The inherent FUZZY LOGIC behaviour of the Self Tuned Radio (STR), which mimics hand tuning, yields a potentially fast yet reliable tuning operation
- The level of the incoming signal at which the radio must lock is software programmable
- Two programmable ports
- High selectivity with distributed IF gain
- Soft mute
- Signal dependent stereo-blend
- High impedance MOSFET input on AM
- Wide supply voltage range of 2.5 to 12 V
- Low current consumption 18 mA at AM and FM (including tuning synthesizer)
- High input sensitivity
- Low output distortion
- Due to the new tuning concept, the tuning is independent of the channel spacing.

GENERAL DESCRIPTION

The TEA5757; TEA5759 is a 44-pin integrated AM/FM stereo radio circuit including a novel tuning concept. The radio part is based on the TEA5712.

The TEA5757 is used in FM-standards in which the local oscillator frequency is above the radio frequency (e.g. european and american standards).

The TEA5759 is the version in which the oscillator frequency is below the radio frequency (e.g. japanese standard).

The new tuning concept combines the advantages of hand tuning with electronic facilities and features. User 'intelligence' is incorporated into the tuning algorithm and an improvement of the analog signal processing is used for the AFC function.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA5757H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2
TEA5759H			

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC1}	supply voltage		2.5	–	12	V
V_{CC2}	supply voltage for tuning		–	–	12	V
V_{tune}	tuning voltage		0.7	–	$V_{CC2} - 0.75$	V
I_{CC1}	supply current	AM mode	12	15	18	mA
		FM mode	13	16	19	mA
I_{DD}	supply current	AM mode	–	3.3	–	mA
		FM mode	–	2.7	–	mA
I_{CC2}	supply current for tuning in preset mode (band-end to band-end)		–	–	640	µA
T_{amb}	operating ambient temperature		−15	–	+60	°C
AM performance; note 1						
V_{10}	AF output voltage	V_{i1} = 5 mV	36	45	70	mV
V_{i1}	RF sensitivity input voltage	S/N = 26 dB	40	55	70	µV
THD	total harmonic distortion	V_{i1} = 1 mV	–	0.8	2.0	%
FM performance; note 2						
V_{10}	AF output voltage	V_{i5} = 5 mV	40	48	57	mV
V_{i5}	RF sensitivity input voltage	V_{10} = −3 dB; V_{10} = 0 dB at V_{i5} = 1 mV	0.4	1.2	3.8	µV
THD	total harmonic distortion	IF filter SFE10.7MS3A20K-A	–	0.3	0.8	%
MPX performance; note 3						
α_{cs}	channel separation		26	30	–	dB

Notes

1. V_{CC1} = 3 V; V_{CC2} = 12 V; V_{DDD} = 3 V; f_i = 1 MHz; m = 0.3; f_m = 1 kHz; measured in Fig.9 with S1 in position A; S2 in position B; unless otherwise specified.
2. V_{CC1} = 3 V; V_{CC2} = 12 V; V_{DDD} = 3 V; f_i = 100 MHz; Δf_m = 22.5 kHz; f_m = 1 kHz; measured in Fig.9 with S2 in position A; S3 in position A and S5 in position A; unless otherwise specified.
3. V_{CC1} = 3 V; V_{CC2} = 12 V; V_{DDD} = 3 V; $V_{in3(L+R)}$ = 155 mV; V_{pilot} = 15.5 mV; f_i = 1 kHz; measured in Fig.9 with S2 in position B; S3 in position B; unless otherwise specified.

BLOCK DIAGRAM

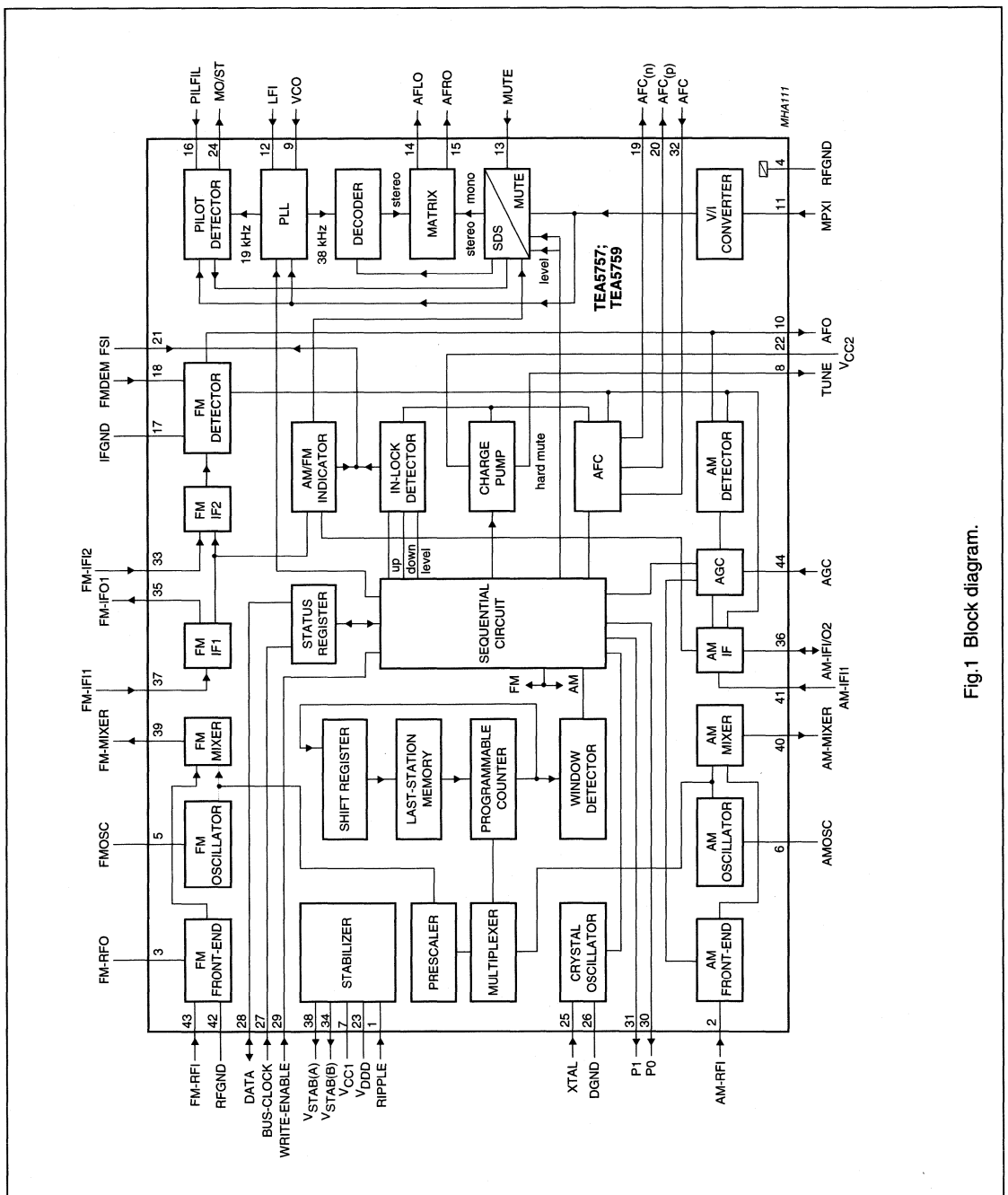


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
RIPPLE	1	ripple capacitor input
AM-RFI	2	AM-RF input
FM-RFO	3	parallel tuned FM-RF circuit to ground
RFGND	4	RF ground and substrate
FMOSC	5	parallel tuned FM-oscillator circuit to ground
AMOSC	6	parallel tuned AM-oscillator circuit to ground
V_{CC1}	7	supply voltage
TUNE	8	tuning output current
VCO	9	voltage controlled oscillator input
AFO	10	AM/FM AF output (output impedance typical 5 kΩ)
MPXI	11	stereo decoder input (input impedance typical 150 kΩ)
LFI	12	loop-filter input
MUTE	13	mute input
AFLO	14	left channel output (output impedance typical 4.3 kΩ)
AFRO	15	right channel output (output impedance typical 4.3 kΩ)
PILFIL	16	pilot detector filter input
IFGND	17	ground of IF, detector and MPX stage
FMDEM	18	ceramic discriminator input
$AFC_{(n)}$	19	AFC negative output
$AFC_{(p)}$	20	AFC positive output
FSI	21	field-strength indicator
V_{CC2}	22	supply voltage for tuning
V_{DDD}	23	digital supply voltage
MO/ST	24	mono/stereo and tuning indication output
XTAL	25	crystal input
DGND	26	digital ground
BUS-CLOCK	27	bus-clock input
DATA	28	bus data input/output
WRITE-ENABLE	29	bus write-enable input
P0	30	programmable output port (P0)
P1	31	programmable output port (P1)
AFC	32	450 kHz LC-input circuit
FM-IFI2	33	FM-IF input 2 (input impedance typical 330 Ω)
$V_{STAB(B)}$	34	internal stabilized supply voltage (B)
FM-IFO1	35	FM-IF output 1 (input impedance typical 330 Ω)
AM-IFI/O2	36	input/output to IFT; output: current source
FM-IFI1	37	FM-IF input 1 (input impedance typical 330 Ω)
$V_{STAB(A)}$	38	internal stabilized supply voltage (A)
FM-MIXER	39	ceramic filter output (output impedance typical 330 Ω)
AM-MIXER	40	open-collector output to IFT

SYMBOL	PIN	DESCRIPTION
AM-IFI1	41	IFT or ceramic filter input (input impedance typical 3 kΩ)
RFGND	42	FM-RF ground
FM-RFI	43	FM-RF aerial input (input impedance typical 40 Ω)
AGC	44	AGC capacitor input

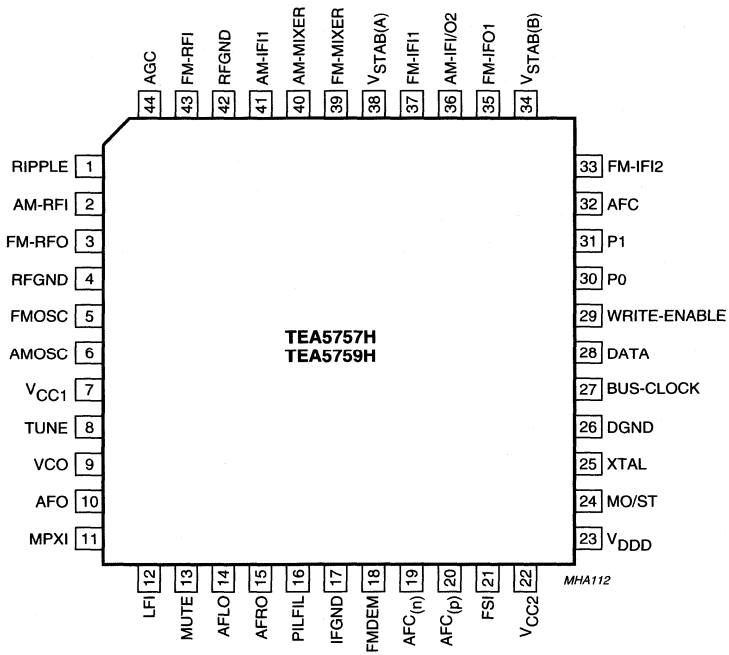


Fig.2 Pin configuration.

Self tuned radio TEA5762

FEATURES

- The tuning system has an optimized IC partitioning both from application (omitting interferences) and flexibility (removable front panel option) point of view: the tuning synthesizer is on-chip with the radio
- The tuning quality is superior and requires no IF counter for stop-detection; it is insensitive to ceramic filter tolerances
- In combination with the microcontroller, fast, low-power operation of preset mode, manual search, automatic search and automatic store are possible
- The local (internal) controller function facilitates reduced and simplified microcontroller software
- The high integration level means fewer external components with regard to the communication between the radio and the microcontroller and a simple and small printed-circuit board (PCB)
- The inherent FUZZY LOGIC behaviour of STR (Self Tuned Radio), which mimics hand tuning, yields a potentially fast yet reliable tuning operation
- The level of the incoming signal at which the radio must lock is software programmable
- Two programmable ports
- FM-on/off port to control the external FM front end
- High selectivity with distributed IF gain
- Soft mute
- Signal dependent stereo-blend
- High impedance MOSFET input on AM
- Wide supply voltage range of 2.5 to 12 V
- Low current consumption 18 mA at AM and FM (including tuning synthesizer for AM)
- Low noise figure
- Low output distortion
- Due to the new tuning concept, the tuning is independent of the channel spacing.

GENERAL DESCRIPTION

The TEA5762 is a 44-pin integrated AM-radio and FM-IF and demodulator part including a novel tuning concept. The radio part is based on the TEA5712.

It is designed for the use with an external FM-front end.

The new tuning concept combines the advantages of hand tuning with electronic facilities and features. User intelligence is incorporated into the tuning algorithm and an improvement of the analog signal processing is used for the AFC function.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA5762H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC1}	supply voltage 1		2.5	–	12	V
V_{CC2}	supply voltage 2 for tuning		–	–	12	V
V_{tune}	tuning voltage		0.7	–	$V_{CC2} - 0.75$	V
I_{CC1}	supply current 1	AM mode	12	15	18	mA
		FM mode	13	16	19	mA
I_{DDD}	digital supply current	AM mode	–	3.3	–	mA
		FM mode	–	2.7	–	mA
I_{CC2}	supply current 2 for tuning in preset mode (band-end to band-end)		–	–	640	µA
T_{amb}	operating ambient temperature		−15	–	+60	°C
AM performance; note 1						
V_{10}	AF output voltage	V_{i1} = 5 mV	36	45	70	mV
V_{i1}	RF sensitivity input voltage	S/N = 26 dB	40	55	70	µV
THD	total harmonic distortion	V_{i1} = 1 mV	–	0.8	2.0	%
FM performance; note 2						
V_{10}	AF output voltage	V_{i4} = 5 mV	40	48	57	mV
V_{i4}	IF sensitivity input voltage	V_{10} = −3 dB; V_{10} = 0 dB at V_{i4} = 10 mV	–	20	30	µV
THD	total harmonic distortion	IF filter SFE10.7MS3A20K-A	–	0.3	0.8	%
MPX performance; note 3						
α_{cs}	channel separation	V_{i4} = 30 mV	26	30	–	dB

Notes

1. Conditions AM: V_{CC1} = 3 V; V_{CC2} = 12 V; V_{DDD} = 3 V; f_i = 1 MHz; m = 0.3; f_m = 1 kHz; measured in Fig.8 with S1 in position A and S2 in position B; unless otherwise specified.
2. Conditions FM: V_{CC1} = 3 V; V_{CC2} = 12 V; V_{DDD} = 3 V; f_i = 10.7 MHz; Δf_m = 22.5 kHz; f_m = 1 kHz; measured in Fig.8 with S2 in position A and S3 in position A; unless otherwise specified.
3. Conditions MPX: V_{CC1} = 3 V; V_{CC2} = 12 V; V_{DDD} = 3 V; $V_{i3(L+R)}$ = 155 mV; V_{pilot} = 15.5 mV; f_i = 1 kHz; measured in with S2 in position B and S3 in position B; unless otherwise specified.

BLOCK DIAGRAM

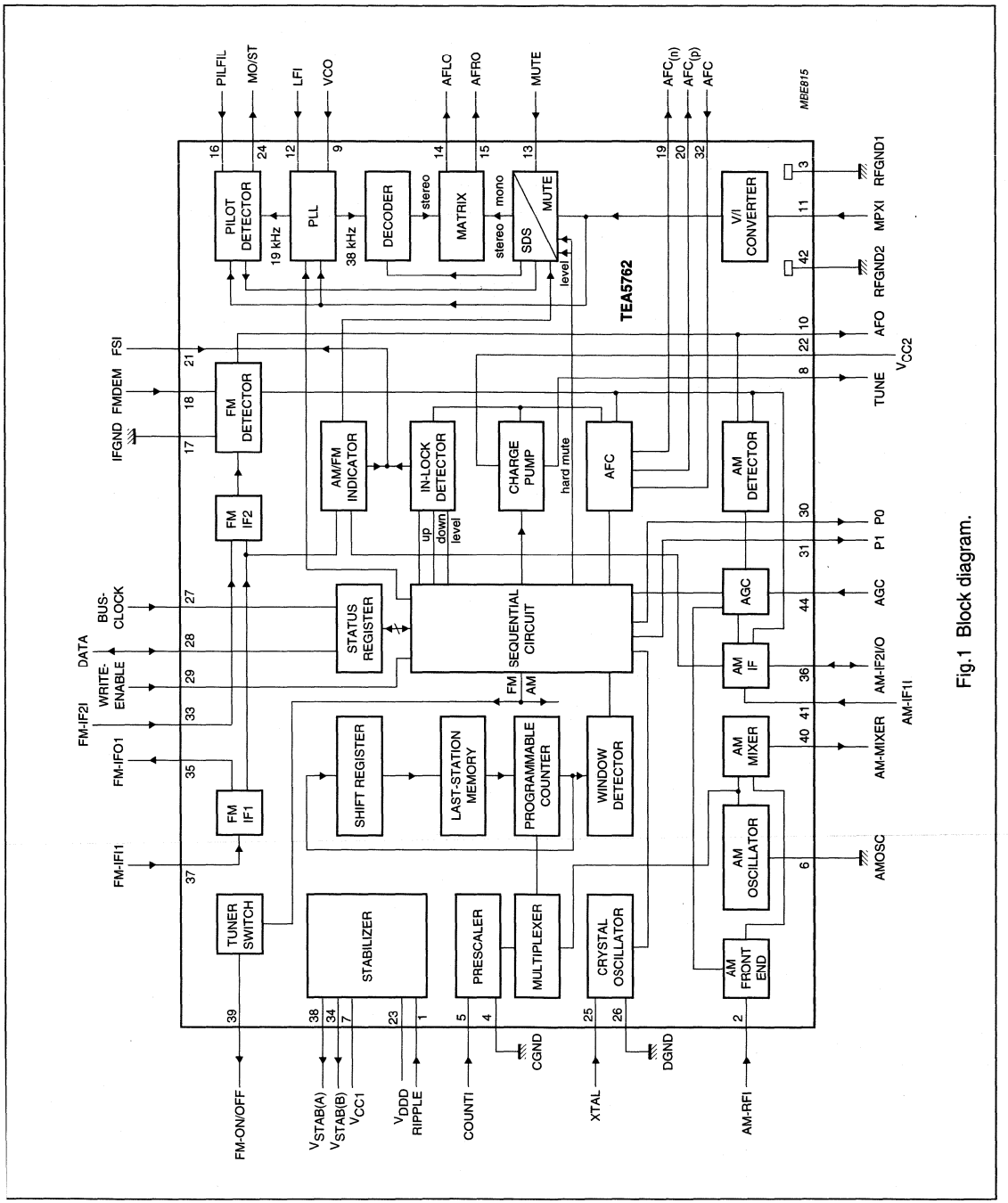


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
RIPPLE	1	ripple capacitor input
AM-RFI	2	AM-RF input
RFGND1	3	RF ground 1 and substrate
CGND	4	counter ground
COUNTI	5	counter input
AMOSC	6	parallel tuned AM oscillator circuit to ground
V_{CC1}	7	supply voltage 1
TUNE	8	tuning output current
VCO	9	voltage controlled oscillator input
AFO	10	AM/FM AF output (output impedance typical 5 kΩ)
MPXI	11	stereo decoder input (input impedance typical 150 kΩ)
LFI	12	loop-filter input
MUTE	13	mute input
AFLO	14	left channel output (output impedance typical 4.3 kΩ)
AFRO	15	right channel output (output impedance typical 4.3 kΩ)
PILFIL	16	pilot detector filter input
IFGND	17	ground of IF, detector and MPX stage
FMDEM	18	ceramic discriminator input
$AFC_{(n)}$	19	AFC negative output
$AFC_{(p)}$	20	AFC positive output
FSI	21	field-strength indicator
V_{CC2}	22	supply voltage 2 (for tuning)
V_{DDD}	23	digital supply voltage
MO/ST	24	mono/stereo and tuning indication output
XTAL	25	crystal input
DGND	26	digital ground
BUS-CLOCK	27	bus-clock input
DATA	28	bus data input/output
WRITE-ENABLE	29	bus write enable input
P0	30	programmable output port (P0)
P1	31	programmable output port (P1)
AFC	32	450 kHz LC input circuit for AM AFC
FM-IF2I	33	FM-IF input 2 (input impedance typical 330 Ω)
$V_{STAB(B)}$	34	internal stabilized supply voltage (B)
FM-IFO1	35	FM-IF output 1 (input impedance typical 330 Ω)
AM-IF2I/O	36	input/output to IFT; output current source
FM-IFI1	37	FM-IF input 1 (input impedance typical 330 Ω)
$V_{STAB(A)}$	38	internal stabilized supply voltage (A)
FM-ON/OFF	39	FM ON/OFF port
AM-MIXER	40	open-collector output to IFT

SYMBOL	PIN	DESCRIPTION
AM-IF1I	41	IFT or ceramic filter input (input impedance typical 3 kΩ)
RFGND2	42	FM-RF ground 2
n.c.	43	not connected
AGC	44	AGC capacitor input

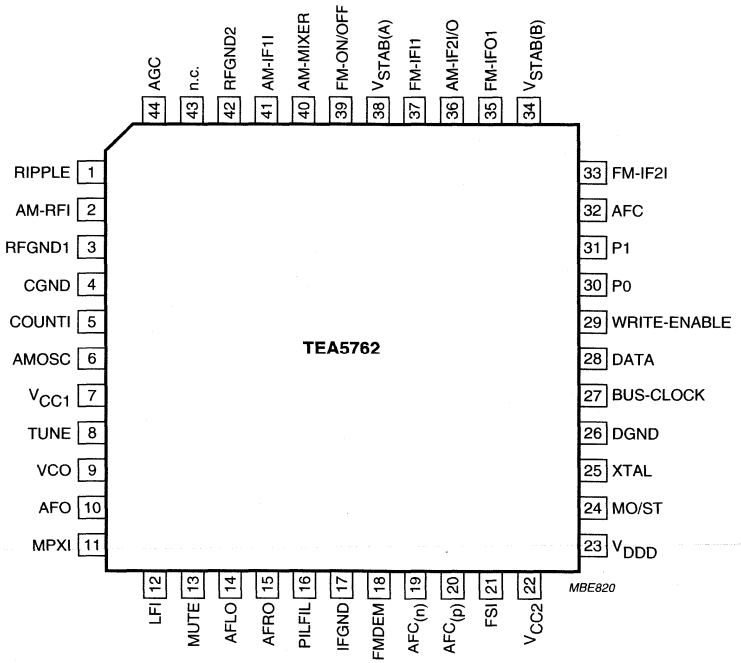


Fig.2 Pin configuration.

Sound fader control circuit TEA6320

FEATURES

- Source selector for four stereo and one mono inputs
- Interface for noise reduction circuits
- Interface for external equalizer
- Volume, balance and fader control
- Special loudness characteristic automatically controlled in combination with volume setting
- Bass and treble control
- Mute control at audio signal zero crossing
- Fast mute control via I²C-bus
- Fast mute control via pin
- I²C-bus control for all functions
- Power supply with internal power-on reset.

GENERAL DESCRIPTION

The sound fader control circuit TEA6320 is an I²C-bus controlled stereo preamplifier for car radio hi-fi sound applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.5	8.5	9.5	V
I_{CC}	supply current	V_{CC} = 8.5 V	–	26	–	mA
$V_{o(rms)}$	maximum output voltage level	V_{CC} = 8.5 V; THD ≤ 0.1%	–	2000	–	mV
G_v	voltage gain		−86	–	+20	dB
$G_{step(vol)}$	step resolution (volume)		–	1	–	dB
G_{bass}	bass control		−15	–	+15	dB
G_{treble}	treble control		−12	–	+12	dB
$G_{step(treble)}$	step resolution (bass, treble)		–	1.5	–	dB
(S+N)/N	signal-plus-noise to noise ratio	V_O = 2.0 V; G_v = 0 dB; unweighted	–	105	–	dB
RR_{100}	ripple rejection	$V_{r(rms)}$ < 200 mV; f = 100 Hz; G_v = 0 dB	–	76	–	dB
α_{cs}	channel separation	250 Hz ≤ f ≤ 10 kHz; G_v = 0 dB	90	96	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6320	SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1
TEA6320T	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

BLOCK DIAGRAM

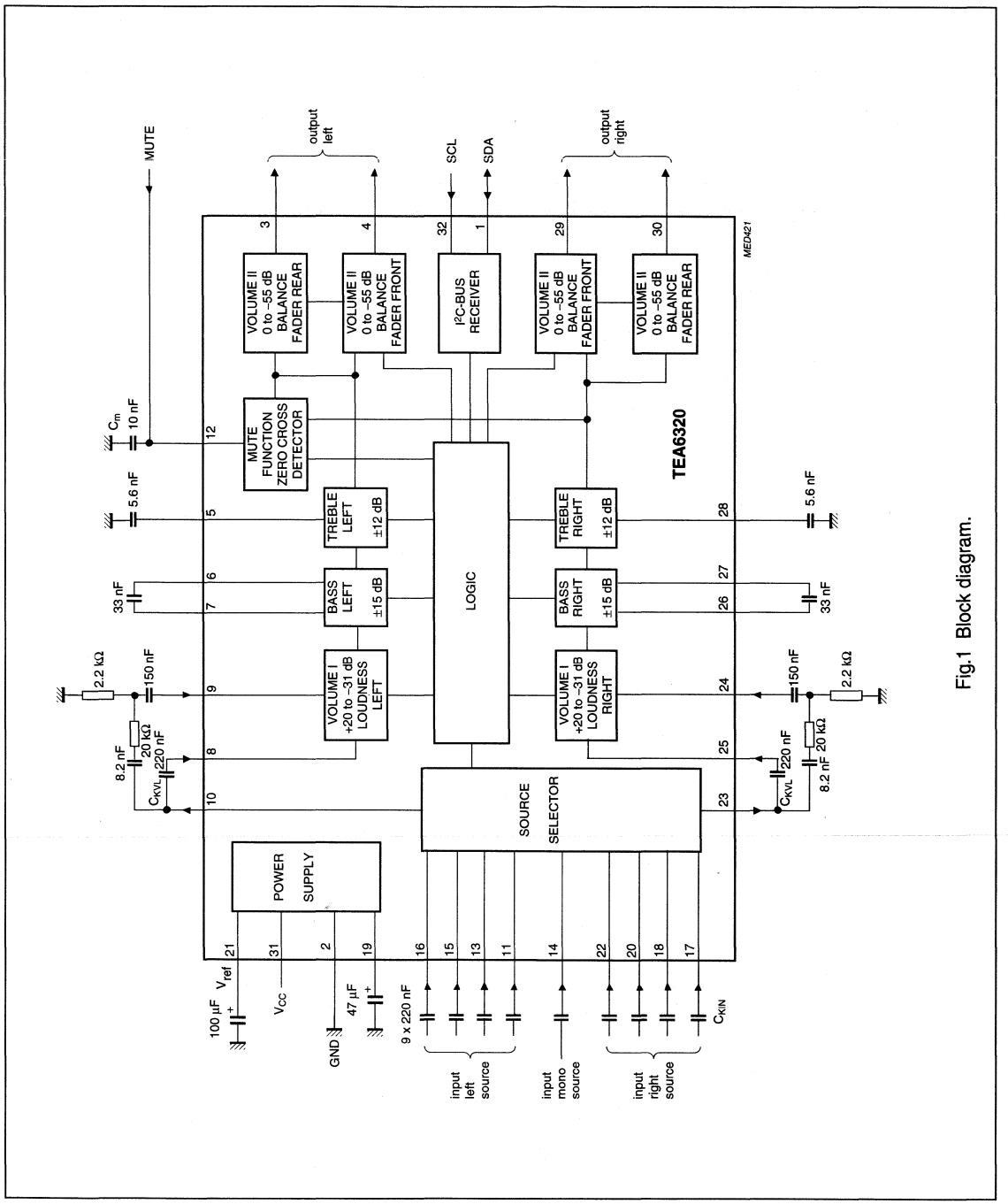


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	serial data input/output
GND	2	ground
OUTLR	3	output left rear
OUTLF	4	output left front
TL	5	treble control capacitor left channel or input from an external equalizer
B2L	6	bass control capacitor left channel or output to an external equalizer
B1L	7	bass control capacitor, left channel
IVL	8	input volume I, left control part
ILL	9	input loudness, left control part
QSL	10	output source selector, left channel
IDL	11	input D left source
MUTE	12	mute control
ICL	13	input C left source
IMO	14	input mono source
IBL	15	input B left source
IAL	16	input A left source
IAR	17	input A right source
IBR	18	input B right source
CAP	19	electronic filtering for supply
ICR	20	input C right source
V_{ref}	21	reference voltage ($0.5V_{CC}$)
IDR	22	input D right source
QSR	23	output source selector right channel
ILR	24	input loudness right channel
IVR	25	input volume I, right control part
B1R	26	bass control capacitor right channel
B2R	27	bass control capacitor right channel or output to an external equalizer
TR	28	treble control capacitor right channel or input from an external equalizer
OUTRF	29	output right front
OUTRR	30	output right rear
V_{CC}	31	supply voltage
SCL	32	serial clock input

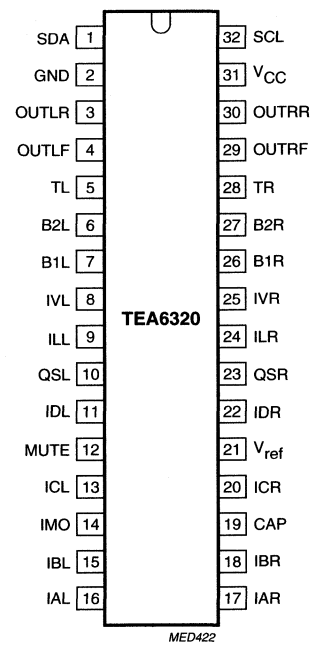


Fig.2 Pin configuration.

Sound fader control circuit TEA6321

FEATURES

- Source selector for four stereo and one mono inputs
- Interface for noise reduction circuits
- Interface for external equalizer
- Volume, balance and fader control
- Special loudness characteristic automatically controlled in combination with volume setting
- Bass control with equalizer filters
- Treble control
- Mute control at audio signal zero crossing
- Fast mute control via I²C-bus
- Fast mute control via pin
- I²C-bus control for all functions
- Power supply with internal power-on reset.

GENERAL DESCRIPTION

The sound fader control circuit TEA6321 is an I²C-bus controlled stereo preamplifier for car radio hi-fi sound applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.5	8.5	9.5	V
I_{CC}	supply current	V_{CC} = 8.5 V	–	26	–	mA
$V_{o(rms)}$	maximum output voltage level	V_{CC} = 8.5 V; THD ≤ 0.1%	–	2000	–	mV
G_v	voltage gain		−86	–	+20	dB
$G_{step(vol)}$	step resolution (volume)		–	1	–	dB
G_{bass}	bass control		−18	–	+18	dB
G_{treble}	treble control		−12	–	+12	dB
$G_{step(treble)}$	step resolution (treble)		–	1.5	–	dB
(S+N)/N	signal-plus-noise to noise ratio	V_o = 2.0 V; G_v = 0 dB; unweighted	–	105	–	dB
RR_{100}	ripple rejection	$V_{r(rms)}$ < 200 mV; f = 100 Hz; G_v = 0 dB	–	75	–	dB
α_{cs}	channel separation	250 Hz ≤ f ≤ 10 kHz; G_v = 0 dB	90	96	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6321T	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

BLOCK DIAGRAM

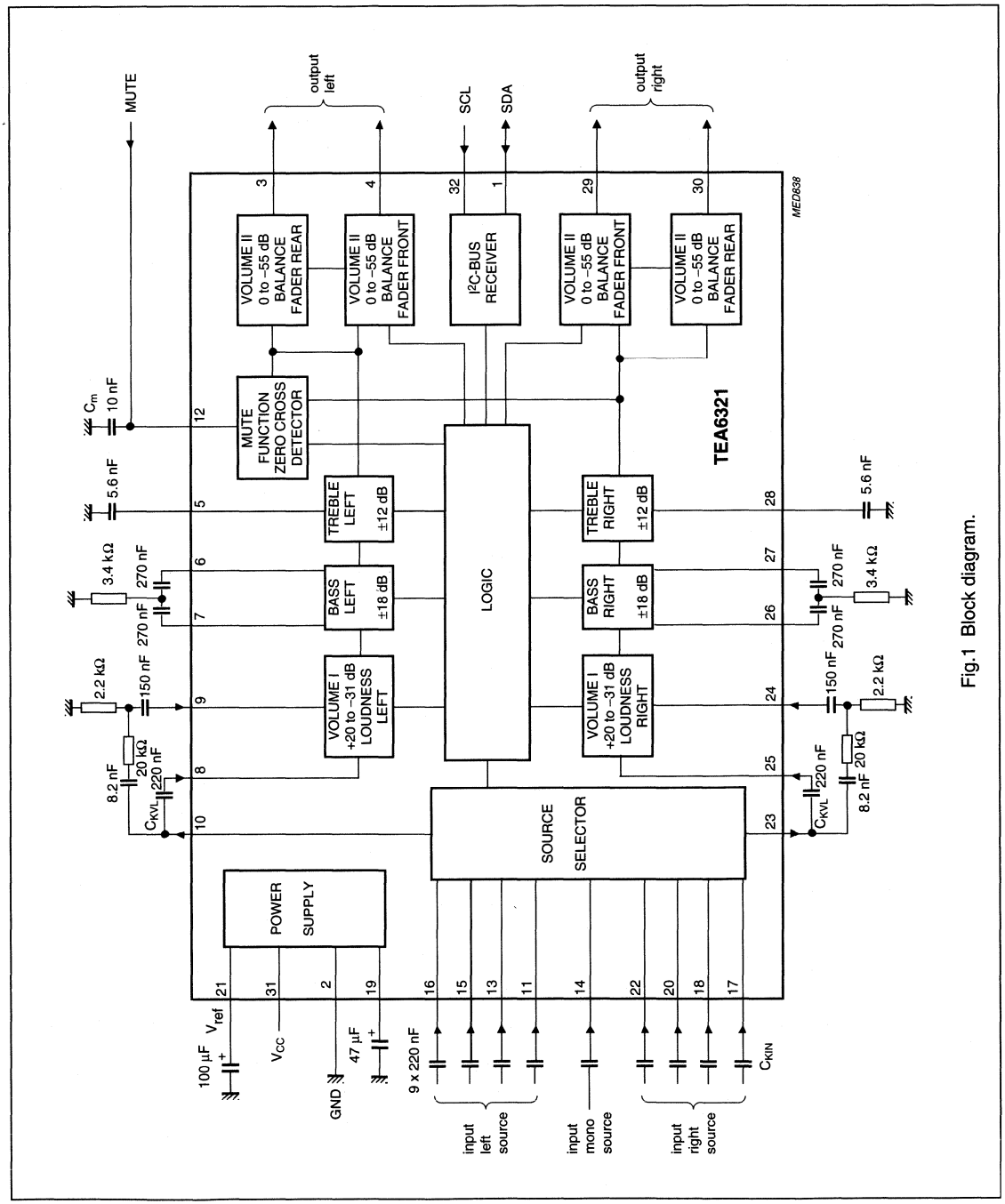


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	serial data input/output
GND	2	ground
OUTLR	3	output left rear
OUTLF	4	output left front
TL	5	treble control capacitor left channel or input from an external equalizer
B2L	6	bass control left channel or output to an external equalizer
B1L	7	bass control, left channel
IVL	8	input volume I, left control part
ILL	9	input loudness, left control part
QSL	10	output source selector, left channel
IDL	11	input D left source
MUTE	12	mute control
ICL	13	input C left source
IMO	14	input mono source
IBL	15	input B left source
IAL	16	input A left source
IAR	17	input A right source
IBR	18	input B right source
CAP	19	electronic filtering for supply
ICR	20	input C right source
V_{ref}	21	reference voltage ($0.5V_{CC}$)
IDR	22	input D right source
QSR	23	output source selector right channel
ILR	24	input loudness right channel
IVR	25	input volume I, right control part
B1R	26	bass control right channel
B2R	27	bass control right channel or output to an external equalizer
TR	28	treble control capacitor right channel or input from an external equalizer
OUTRF	29	output right front
OUTRR	30	output right rear
V_{CC}	31	supply voltage
SCL	32	serial clock input

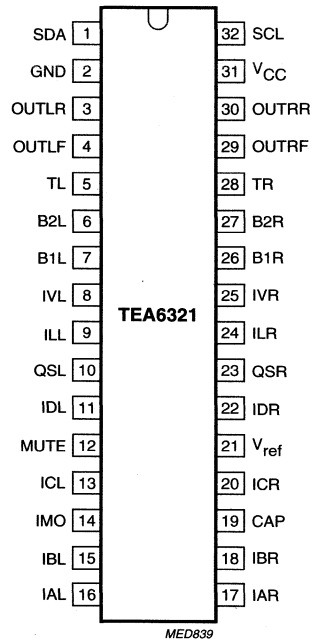


Fig.2 Pin configuration.

Sound fader control circuit TEA6322T

FEATURES

- Source selector for three stereo and one differential stereo input for remote sources
- The differential stereo input works optional as a fourth stereo input and the common mode pin can be used as well as an additional mono input
- Interface for noise reduction circuits
- Interface for external equalizer
- Volume, balance and fader control
- Output at volume I for external booster
- Special loudness characteristic automatically controlled in combination with volume setting
- Bass and treble control
- Mute control at audio signal zero crossing
- Logic output to read mute status
- Fast mute control via I²C-bus
- Fast mute control via pin
- I²C-bus control for all functions
- Power supply with internal power-on reset
- Power-down indication.

GENERAL DESCRIPTION

The sound fader control circuit TEA6322T is an I²C-bus controlled stereo preamplifier for car radio hi-fi sound applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.5	8.5	9.5	V
I_{CC}	supply current	V_{CC} = 8.5 V	–	26	–	mA
$V_{o(rms)}$	maximum output voltage level	V_{CC} = 8.5 V; THD ≤ 0.1%	–	2000	–	mV
G_v	voltage gain		–86	–	+20	dB
$G_{step(vol)}$	step resolution (volume)		–	1	–	dB
G_{bass}	bass control		–15	–	+15	dB
G_{treble}	treble control		–12	–	+12	dB
$G_{step(treble)}$	step resolution (bass, treble)		–	1.5	–	dB
(S+N)/N	signal-plus-noise to noise ratio	V_O = 2.0 V; G_v = 0 dB; unweighted	–	105	–	dB
RR_{100}	ripple rejection	$V_{r(rms)}$ < 200 mV; f = 100 Hz; G_v = 0 dB	–	75	–	dB
CMRR	common mode rejection ratio differential stereo input		43	53	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6322T	VSO40	plastic very small outline package; 40 leads	SOT158-1

BLOCK DIAGRAM

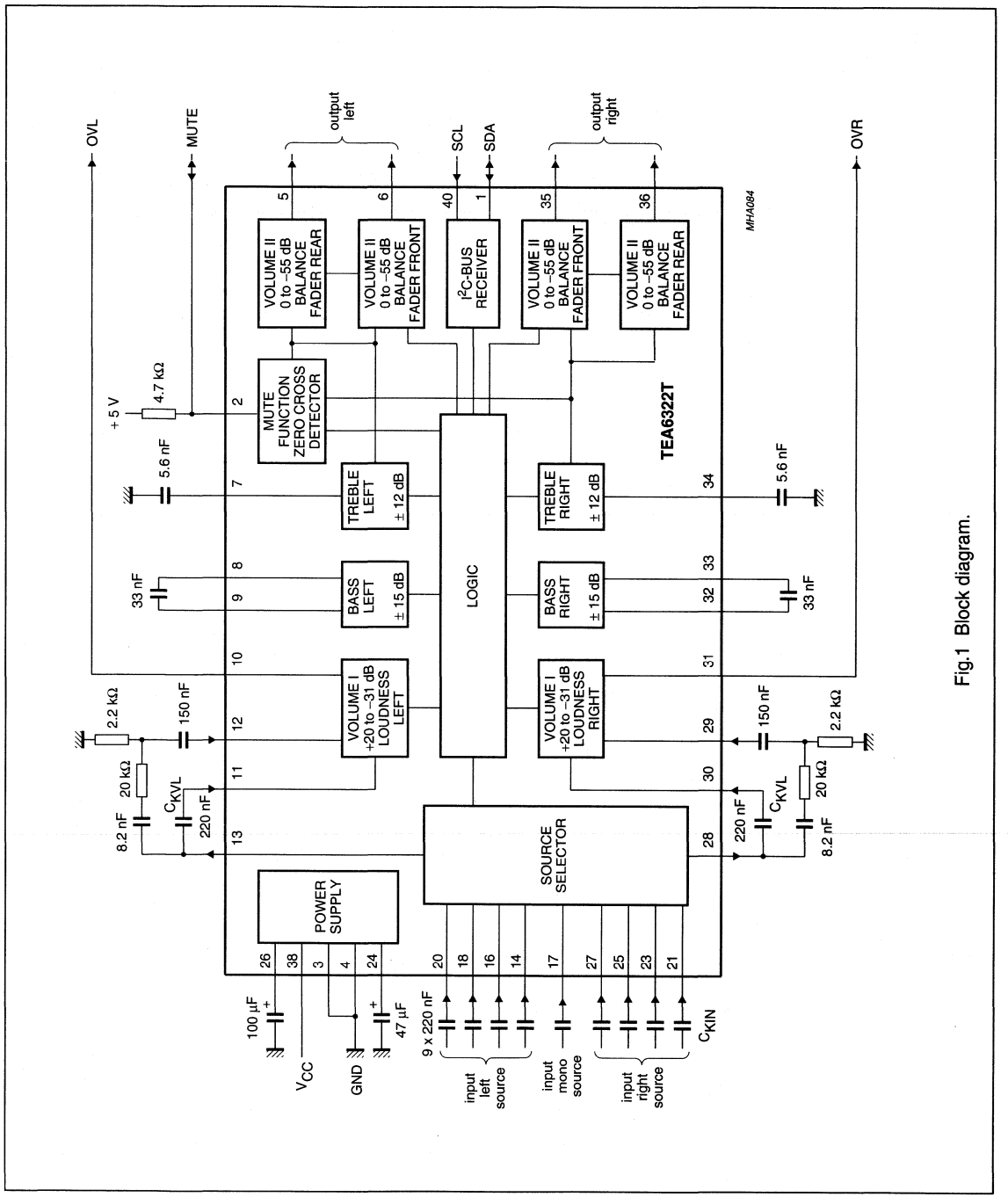


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	serial data input/output
MUTE	2	mute control input and output
DGND	3	digital ground
AGND	4	analog ground
OUTLR	5	output left rear
OUTLF	6	output left front
TL	7	treble control capacitor left channel or input from external equalizer
B2L	8	bass control capacitor left channel or output to an external equalizer
B1L	9	bass control capacitor, left channel
OVL	10	output volume I, left channel
IVL	11	input volume I, left control part
ILL	12	input loudness, left control part
QSL	13	output source selector, left channel
IDL	14	input D left source
i.c.	15	COMM, common mode rejection adjust, centre position
ICL	16	input C left source
COM	17	common mode input / mono source input
IBL	18	input B left source
i.c.	19	COML, common mode rejection adjust, left position
IAL	20	input A differential source left
IAR	21	input A differential source right
i.c.	22	COMR, common mode rejection adjust, right position
IBR	23	input B right source
CAP	24	electronic filtering for supply
ICR	25	input C right source
V_{ref}	26	reference voltage (0.5 V_{CC})
IDR	27	input D right source
QSR	28	output source selector right channel
ILR	29	input loudness right channel
IVR	30	input volume I, right control part
OVR	31	output volume I, right channel
B1R	32	bass control capacitor right channel
B2R	33	bass control capacitor right channel or output to an external equalizer
TR	34	treble control capacitor right channel or input from an external equalizer
OUTRF	35	output right front
OUTRR	36	output right rear
n.c.	37	not connected
V_{CC}	38	supply voltage
n.c.	39	not connected
SCL	40	serial clock input

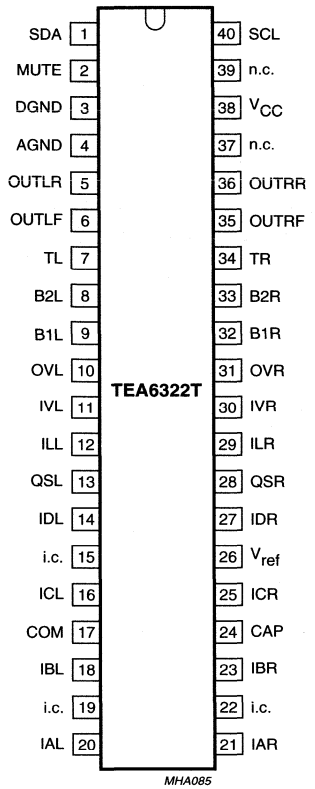


Fig.2 Pin configuration.

Sound fader control circuit TEA6323T

FEATURES

- Source selector for three stereo and one differential stereo input for remote sources
- The differential stereo input works optional as a fourth stereo input and the common mode pin can be used as well as an additional mono input
- Interface for noise reduction circuits
- Interface for external equalizer
- Volume, balance and fader control
- Output at volume I for external booster
- Special loudness characteristic automatically controlled in combination with volume setting
- Bass control with equalizer filters
- Treble control
- Mute control at audio signal zero crossing
- Logic output to read mute status
- Fast mute control via I²C-bus
- Fast mute control via pin
- I²C-bus control for all functions
- Power supply with internal power-on reset
- Power down indication.

GENERAL DESCRIPTION

The sound fader control circuit TEA6323T is an I²C-bus controlled stereo preamplifier for car radio hi-fi sound applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.5	8.5	9.5	V
I_{CC}	supply current	V_{CC} = 8.5 V	–	26	–	mA
$V_{o(rms)}$	maximum output voltage level	V_{CC} = 8.5 V; THD ≤ 0.1%	–	2000	–	mV
G_v	voltage gain		–86	–	+20	dB
$G_{step(vol)}$	step resolution (volume)		–	1	–	dB
G_{bass}	bass control		–18	–	+18	dB
G_{treble}	treble control		–12	–	+12	dB
$G_{step(treble)}$	step resolution (treble)		–	1.5	–	dB
(S+N)/N	signal-plus-noise to noise ratio	V_O = 2.0 V; G_v = 0 dB; unweighted	–	105	–	dB
RR_{100}	ripple rejection	$V_{r(rms)}$ < 200 mV; f = 100 Hz; G_v = 0 dB	–	75	–	dB
CMRR	common mode rejection ratio differential stereo input		43	53	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6323T	VSO40	plastic very small outline package; 40 leads	SOT158-1

BLOCK DIAGRAM

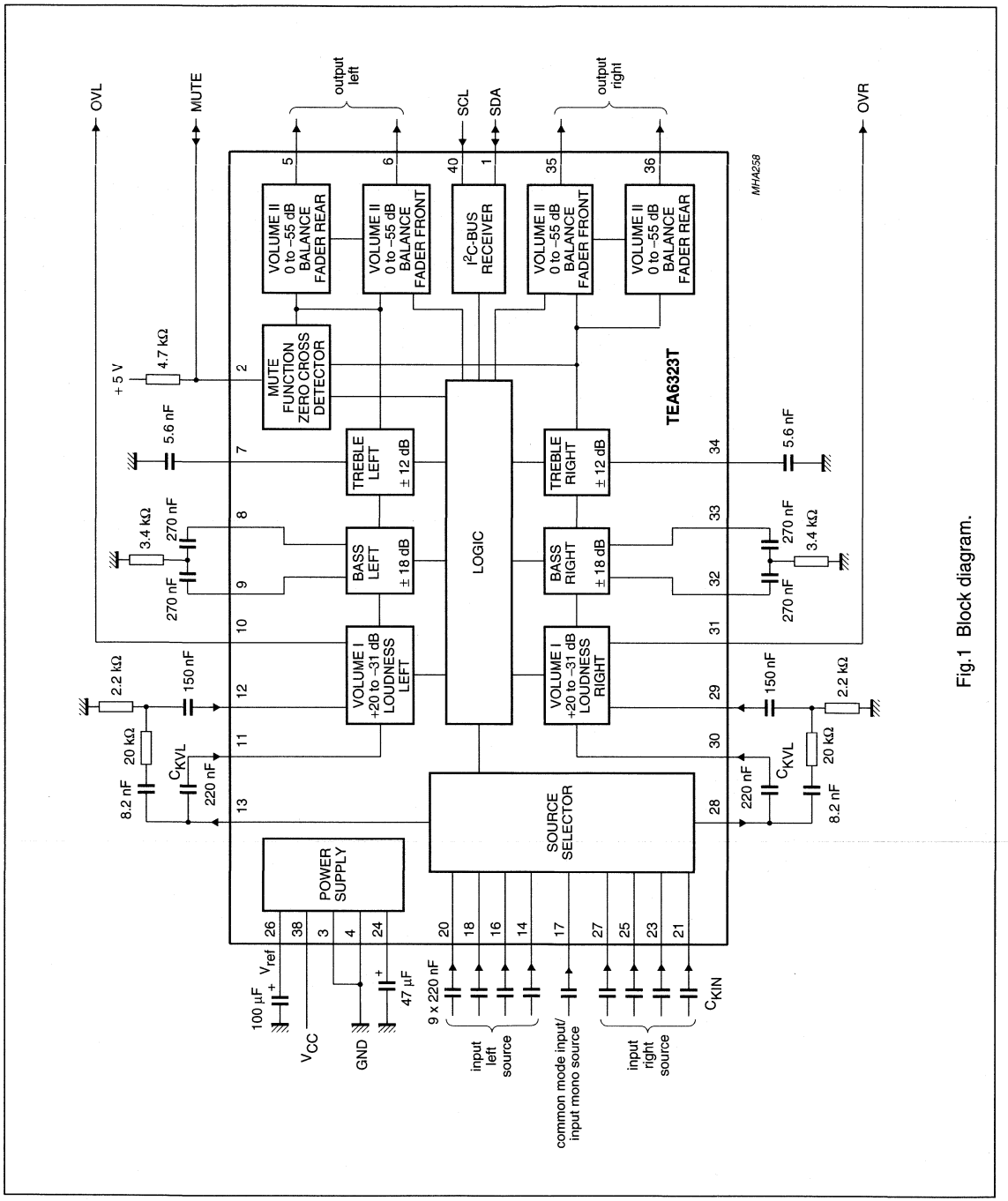


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	serial data input/output
MUTE	2	mute control input and output
DGND	3	digital ground
AGND	4	analog ground
OUTLR	5	output left rear
OUTLF	6	output left front
TL	7	treble control capacitor left channel or input from an external equalizer
B2L	8	bass control left channel or output to an external equalizer
B1L	9	bass control, left channel
OVL	10	output volume I, left channel
IVL	11	input volume I, left control part
ILL	12	input loudness, left control part
QSL	13	output source selector, left channel
IDL	14	input D left source
i.c.	15	COMM, common mode rejection adjust, centre position
ICL	16	input C left source
COM	17	common mode input / mono source input
IBL	18	input B left source
i.c.	19	COML, common mode rejection adjust, left position
IAL	20	input A differential source left
IAR	21	input A differential source right
i.c.	22	COMR, common mode rejection adjust, right position
IBR	23	input B right source
CAP	24	electronic filtering for supply
ICR	25	input C right source
V_{ref}	26	reference voltage ($0.5V_{CC}$)
IDR	27	input D right source
QSR	28	output source selector right channel
ILR	29	input loudness right channel
IVR	30	input volume I, right control part
OVR	31	output volume I, right channel
B1R	32	bass control right channel
B2R	33	bass control right channel or output to an external equalizer
TR	34	treble control capacitor right channel or input from an external equalizer
OUTRF	35	output right front
OUTRR	36	output right rear
n.c.	37	not connected
V_{CC}	38	supply voltage
n.c.	39	not connected
SCL	40	serial clock input

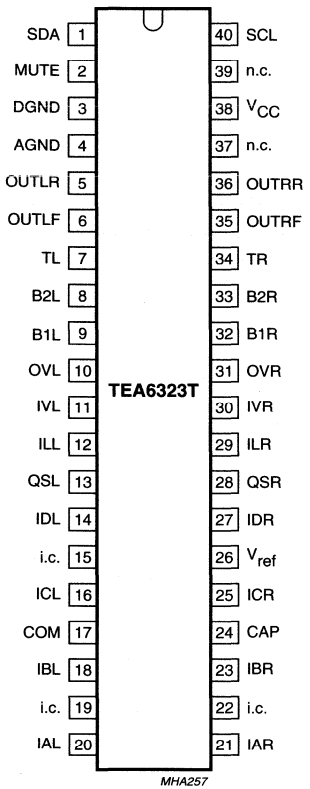


Fig.2 Pin configuration.

5-band stereo equalizer circuit TEA6360

FEATURES

- Monolithic integrated 5-band stereo equalizer circuit
- Five filters for each channel
- Centre frequency, bandwidth and maximum boost/cut defined by external components
- Choise for variable or constant Q-factor via I²C software
- Defeat mode
- All stages are DC-coupled
- I²C-bus control for all functions
- Two different modul addresses programmable.

GENERAL DESCRIPTION

The 5-band stereo equalizer is an 1²C-bus controlled tone processor for application in car radio sets, TV sets and music centres. It offers the possibility of sound control as well as equalization of sound pressure behaviour of different rooms or loudspeakers, especially in cars.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_p	supply voltage (pin 14)	7	8.5	13.2	V
I_p	supply current	–	24.5	–	mA
$V_{1,32}$	input voltage range	–	2.1 to V_{P-1}	–	V
V_o	maximum output signal level (RMS value, pins 13 and 20)	- 1.1		–	V
G_v	total signal gain, all filters linear	–0.5	–	0	dB
B	–1 dB frequency response (linear)	0 to 20	–	–	kHz
T_{amb}	operating ambient temperature	–40	–	85	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA6360[1]	32	shrink DIL	plastic	SOT232
TEA6360/T[2]	32	mini-pack	plastic	SOT287

Notes

1. SOT232; SOT232-1; 1996 August 08.
2. SOT287; SOT287-1; 1996 August 08.

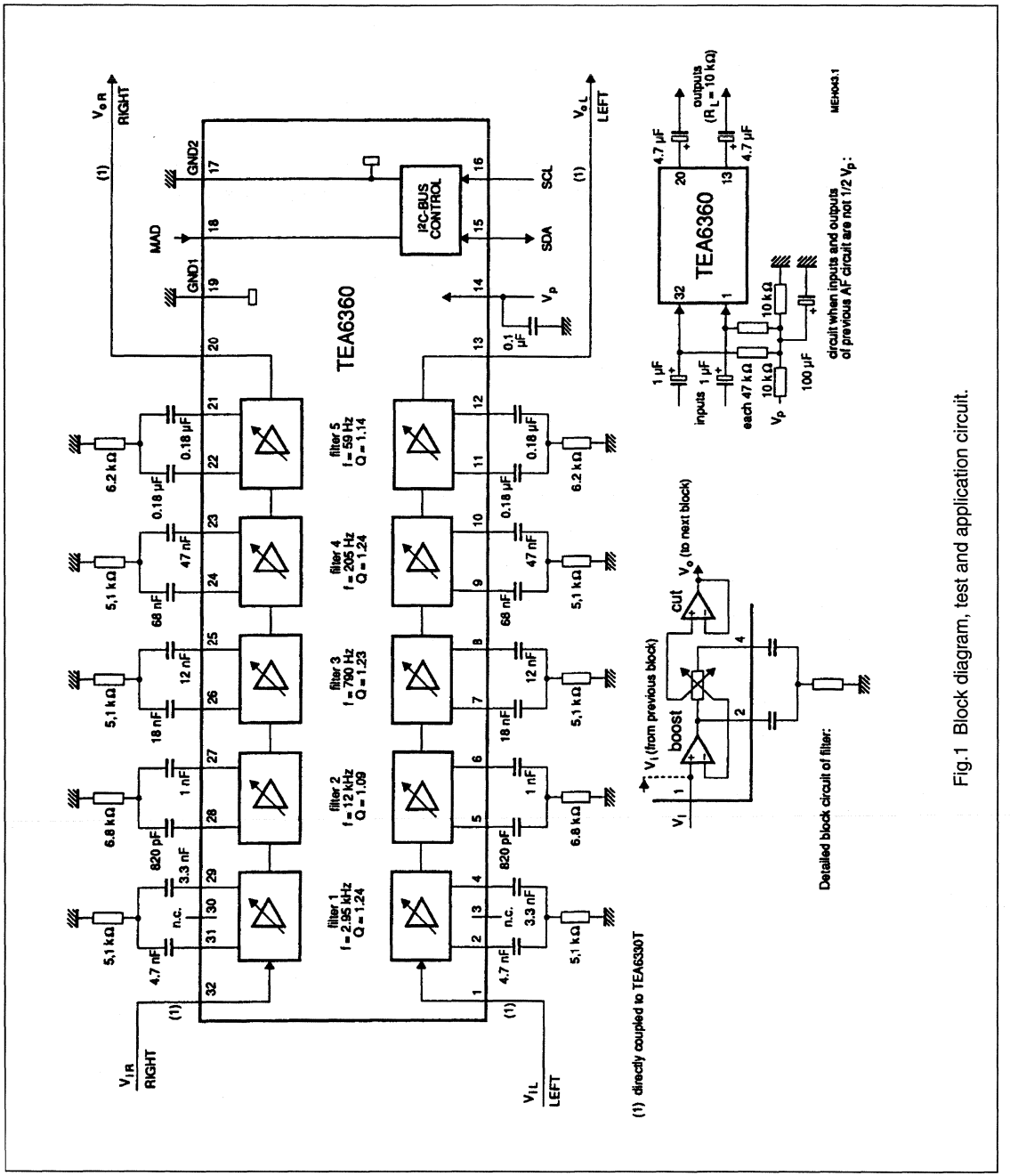


Fig.1 Block diagram, test and application circuit.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{iL}	1	audio frequency input LEFT
F1LA	2	connection A for filter 1 LEFT (f = 2.95 kHz)
n.c.	3	not connected
F1LB	4	connection B for filter 1 LEFT (f = 2.95 kHz)
F2LA	5	connection A for filter 2 LEFT (f = 12 kHz)
F2LB	6	connection B for filter 2 LEFT (f = 12 kHz)
F3LA	7	connection A for filter 3 LEFT (f = 790 Hz)
F3LB	8	connection B for filter 3 LEFT (f = 790 Hz)
F4LA	9	connection A for filter 4 LEFT (f = 205 Hz)
F4LB	10	connection B for filter 4 LEFT (f = 205 Hz)
F5LA	11	connection A for filter 5 LEFT (f = 59 Hz)
F5LB	12	connection B for filter 5 LEFT (f = 59 Hz)
V_{oL}	13	audio frequency output LEFT
V_P	14	supply voltage (+8.5 V)
SDA	15	I²C-bus data line
SCL	16	I²C-bus clock line
GND2	17	ground 2 (I²C-bus ground)
MAD	18	modul address
GND1	19	ground 1 (analog ground)
V_{oR}	20	audio frequency output RIGHT
F5RB	21	connection B for filter 5 RIGHT (f = 59 Hz)
F5RA	22	connection A for filter 5 RIGHT (f = 59 Hz)
F4RB	23	connection B for filter 4 RIGHT (f = 205 Hz)
F4RA	24	connection A for filter 4 RIGHT (f = 205 Hz)
F3RB	25	connection B for filter 3 RIGHT (f = 790 Hz)
F3RA	26	connection A for filter 3 RIGHT (f = 790 Hz)
F2RB	27	connection B for filter 2 RIGHT (f = 12 kHz)
F2RA	28	connection A for filter 2 RIGHT (f = 12 kHz)
F1RB	29	connection B for filter 1 RIGHT (f = 2.95 kHz)
n.c.	30	not connected
F1RA	31	connection A for filter 1 RIGHT (f = 2.95 kHz)
V_{iR}	32	audio frequency input RIGHT

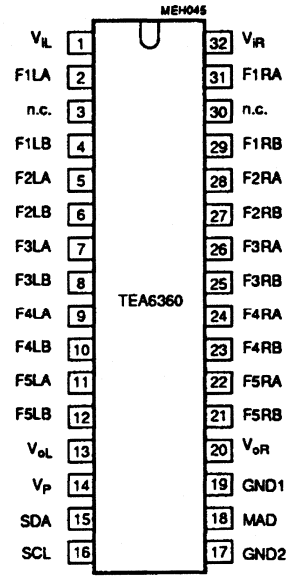


Fig.2 Pin configuration

Front-end and PLL synthesizers for car radios

TEA6810V; TEA6811V

:EATURES

Synthesizer function which includes a Voltage Controlled Oscillator (VCO), dividers, phase detector, charge-pump and in-lock detector

FM mixer with AGC

AM RF amplifier with AGC

AM mixer.

\PPLICATIONS

Car radios.

;ENERAL DESCRIPTION

'he TEA6810V and TEA6811V, together with TEA6821V)rms an AM/FM receiving concept for electronically tuned ar radios.

'he TEA681xV is an FM/AM front-end with one local ynthesized oscillator for both AM and FM which is used)gether with the TEA6821T in a double-conversion oncept. It delivers a first FM-IF of 72.2 MHz and, for 1W/LW, a first AM-IF of 10.7 MHz.

Minimum alignments are required due to wideband RF inputs and the common AM/FM VCO.

High dynamic behaviour and minimum distortion is obtained by a special RF input design combined with AGC. High sensitivity is possible in combination with RF input FETs.

Minimum interference is experienced due a to special synthesizer loop design and ensuring that the I²C-bus is inoperative in the locked-tuned condition.

The reference frequency for the synthesizer and the I²C-bus information is delivered by the TEA6821V.

The programmable local/dx switch enables switching the gain of the FM mixer from normal AGC control (FM dx) to the forced 4th level of AGC (FM local).

1UICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA1}	analog supply voltage (pin 2)		4.75	5.0	5.25	V
V_{CCA2}	analog supply voltage (pin 13)		8.1	8.5	8.9	V
V_{AMant}	AM AGC range	see Fig.4	0.3	–	6.0	V
V_{FMant}	FM AGC range	see	10	–	600	mV
f_{AMant}	AM input frequency		0.144	–	22	MHz
f_{FMant}	FM input frequency		60	–	108	MHz
T_{amb}	operating ambient temperature		−40	–	+85	°C

)RDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6810V	VSO40	plastic very small outline package; 40 leads	SOT158-1
TEA6811V	VSO40	plastic very small outline package; 40 leads; face down	SOT158-2

BLOCK DIAGRAM

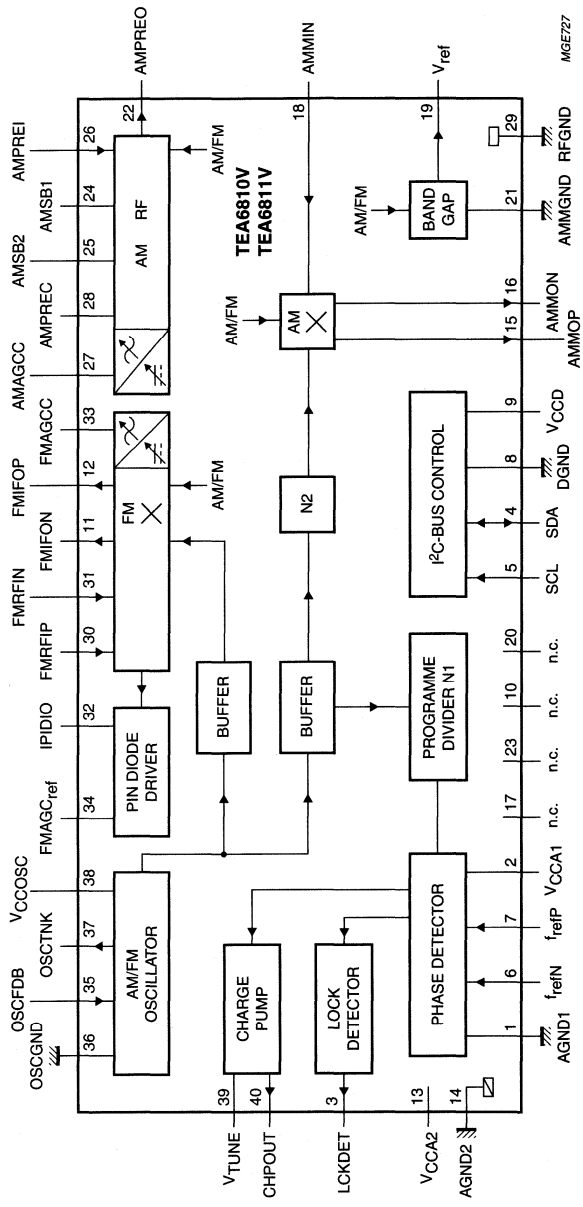


Fig.1 Block diagram.

PINNING

SYMBOL	PIN[1]		DESCRIPTION
	TEA6810	TEA6811	
AGND1	1	1	analog ground 1
V_{CCA1}	2	2	analog supply voltage 1 (+5 V)
LCKDET	3	3	lock detector flag
SDA	4	4	serial data input/output; I^2C-bus
SCL	5	5	serial clock input; I^2C-bus
f_{refN}	6	6	reference frequency input from TEA6821 N-terminal
f_{refP}	7	7	reference frequency input from TEA6821 P-terminal
DGND	8	8	digital ground
V_{CCD}	9	9	digital supply voltage (+5 V)
n.c.	10	10	not connected
FMIFON	11	11	FM mixer negative output (72.2 MHz)
FMIFOP	12	12	FM mixer positive output (72.2 MHz)
V_{CCA2}	13	13	analog supply voltage 2 (+8.5 V)
AGND2	14	14	analog ground 2
AMMOP	15	15	AM mixer positive output (10.7 MHz)
AMMON	16	16	AM mixer negative output (10.7 MHz)
n.c.	17	17	not connected
AMMIN	18	18	AM mixer RF input
V_{ref}	19	19	reference voltage output from AM band gap
n.c.	20	20	not connected
AMMGND	21	21	AM mixer ground
AMPREO	22	22	AM preamplifier output
n.c.	23	23	not connected
AMSB1	24	24	AM feedback switch SB1
AMSB2	25	25	AM feedback switch SB2
AMPREI	26	26	AM preamplifier input
AMAGCC	27	27	AM AGC capacitor
AMPREC	28	28	AM preamplifier decoupling capacitor
RFGND	29	29	RF ground
FMRFIP	30	30	RF positive input for FM mixer
FMRFIN	31	31	RF negative input for FM mixer
IPIDIO	32	32	pin diode drive
FMAGCC	33	33	FM AGC integrating capacitor
$FMAGC_{ref}$	34	34	FM AGC reference voltage
OSCFDB	35	35	oscillator feedback input
OSCGND	36	36	oscillator ground
OSCTNK	37	37	oscillator tank output

SYMBOL	PIN[1]		DESCRIPTION
	TEA6810	TEA6811	
V_{CCOSC}	38	38	oscillator supply voltage (+8.5 V)
V_{TUNE}	39	39	tuning voltage
CHPOUT	40	40	charge pump output

Note

1. Pins 10, 17, 20 and 23 should be connected to a common ground.

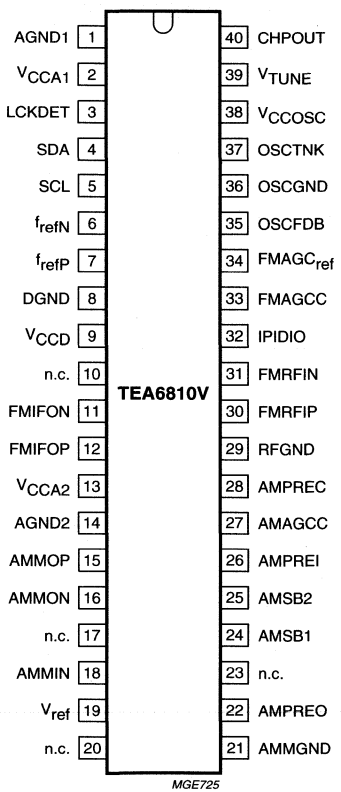


Fig.2 Pin configuration (TEA6810).

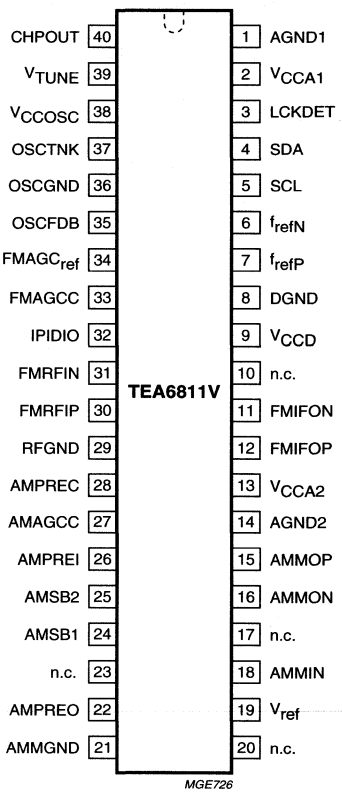


Fig.3 Pin configuration (TEA6811).

ICE car radio TEA6821T

FEATURES

General

- FM mixer for conversion from FM IF_1 = 72.2 MHz to FM IF_2 = 10.7 MHz
- AM mixer for conversion from AM IF_1 = 10.7 MHz to AM IF_2 = 450 kHz
- FM IF gain stage
- Crystal oscillator providing mixer frequencies and references for IF count and stereo decoder
- FM quadrature demodulator with automatic centre frequency adjust and THD compensation
- Level and multipath and noise detectors
- Soft mute
- Stereo noise cancelling and variable de-emphasis
- PLL stereo decoder
- Noise blanker
- AM IF amplifier and demodulator
- I²C-bus transceiver
- IF count for AM and FM
- Reference frequency generation for PLL synthesizer
- Reduced external components
- SW applicable.

Stereo decoder

- Adjustment-free PLL-VCO
- Pilot depending mono/stereo switching
- Analog control of mono/stereo blend
- Adjacent channel noise suppression (114 kHz)
- Pilot canceller
- Analog control of de-emphasis
- Integrated low-pass filters for 190 kHz adjacent channel interferences and signal delay for interference absorption circuit.

GENERAL DESCRIPTION

The TEA6821T together with the TEA6810T / TEA6811T forms an AM/FM electronic tuned car radio in a double conversion receiver concept for European, American and Japanese frequency range.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{s1}	supply voltage 1 (pins 56 and 28)	note 1	7	8.5	10	V
V_{s1}	operating range		8.1	8.5	8.9	V
I_{s1}	supply current 1 FM		–	28	–	mA
I_{s1}	supply current 1 AM		–	24	–	mA
V_{s2}	supply voltage 2 (pin 5)	note 1	4.5	5.0	5.5	V
V_{s2}	operating range		4.75	5.0	5.25	V
I_{s2}	supply current 2 FM		–	31	–	mA
I_{s2}	supply current 2 AM		–	28	–	mA
S+N/N	signal-to-noise AM	m = 0.3	–	57	–	dB
THD	distortion AM		–	1	2	%
S+N/N	signal-to-noise FM	Δf = 22.5 kHz at pins 43 and 47	66	72	–	dB
THD	distortion FM	Δf = 75 kHz	–	0.1	0.35	%
α	channel separation (adjusted)		40	–	–	dB
T_{amb}	operating ambient temperature		–40	–	+85	°C

Note to the quick reference data

1. IC is functional, specified parameters may deviate from limits which are valid for operating range.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6821T	VSO56	plastic very small outline package; 56 leads	SOT190-1

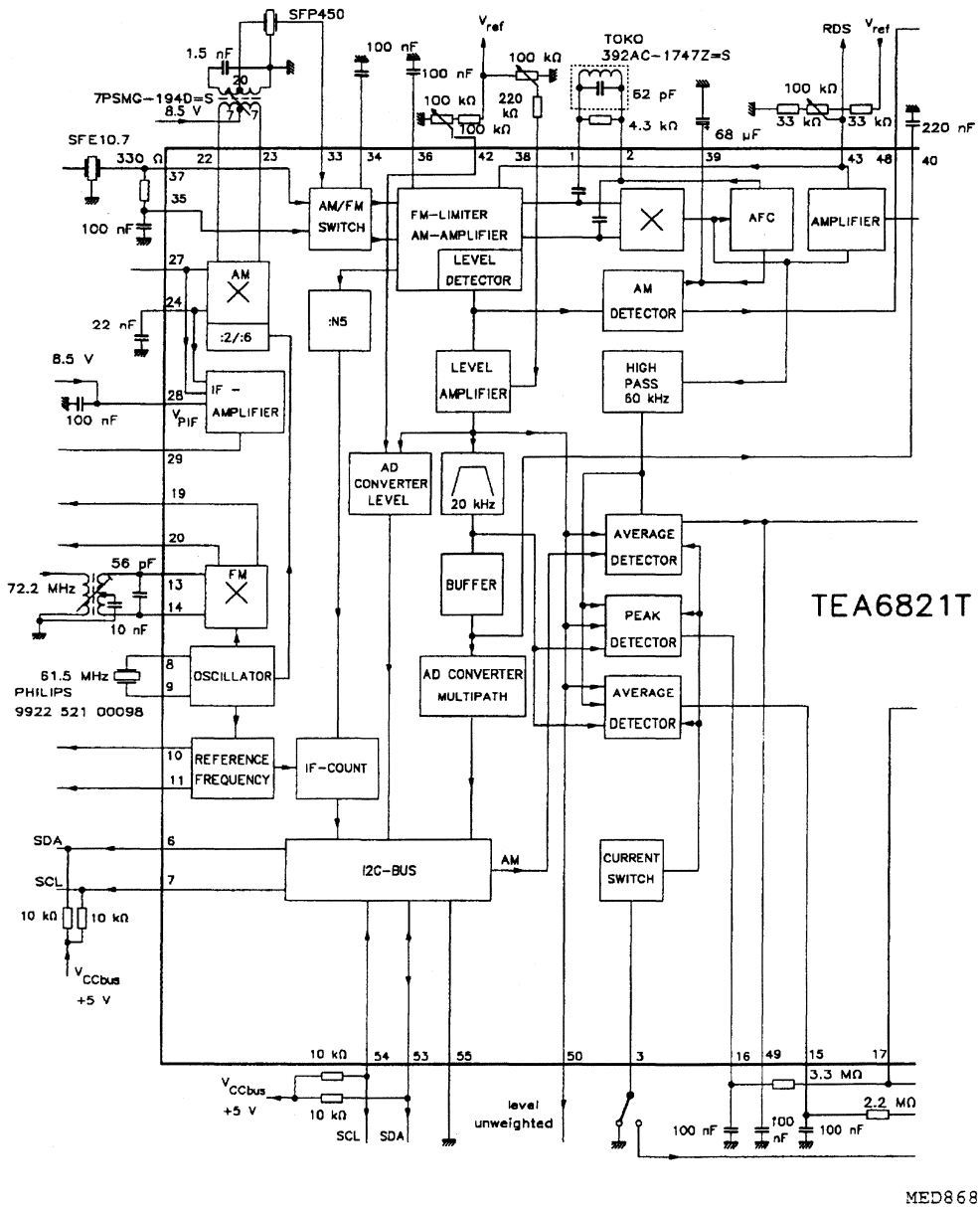


Fig.1 Block diagram (continued in Fig.2).

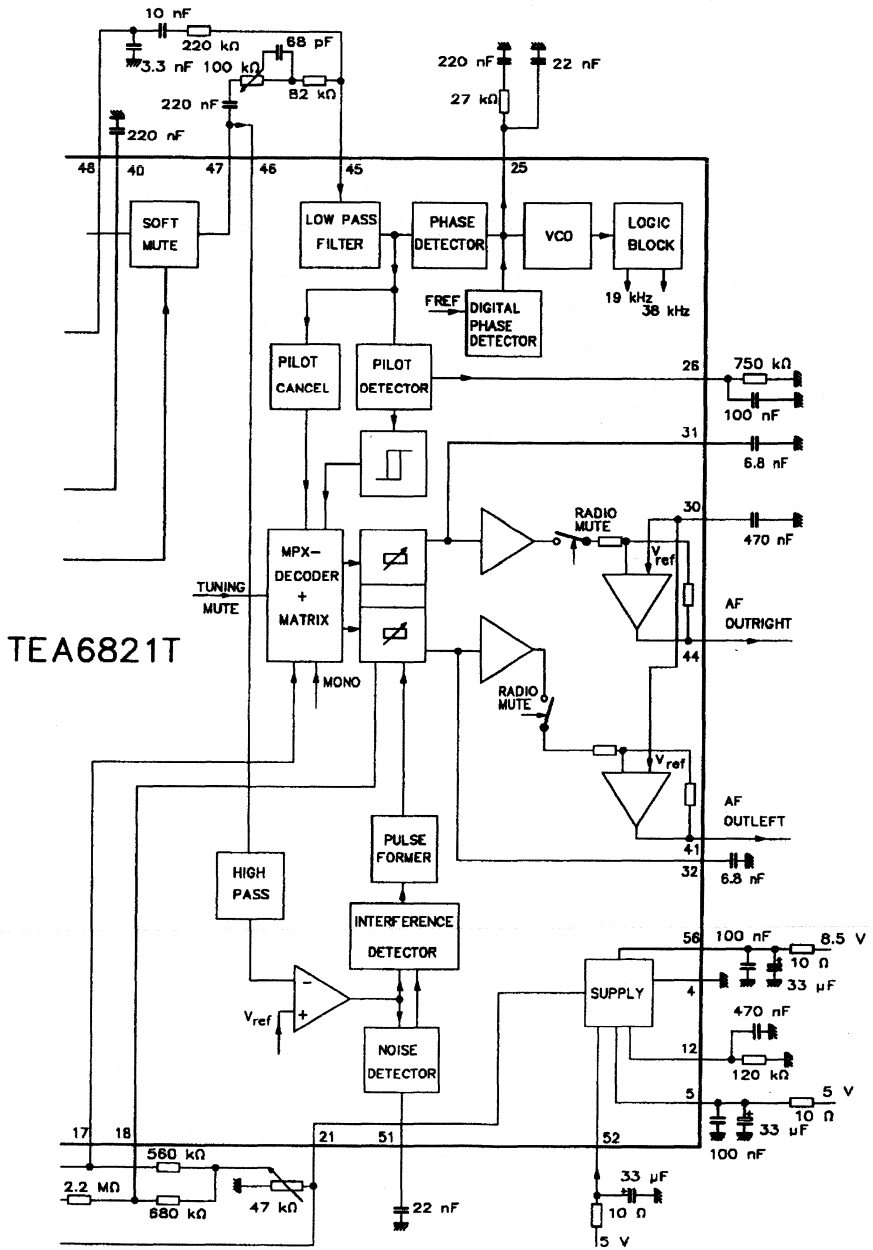


Fig.2 Block diagram (continued from Fig.1).

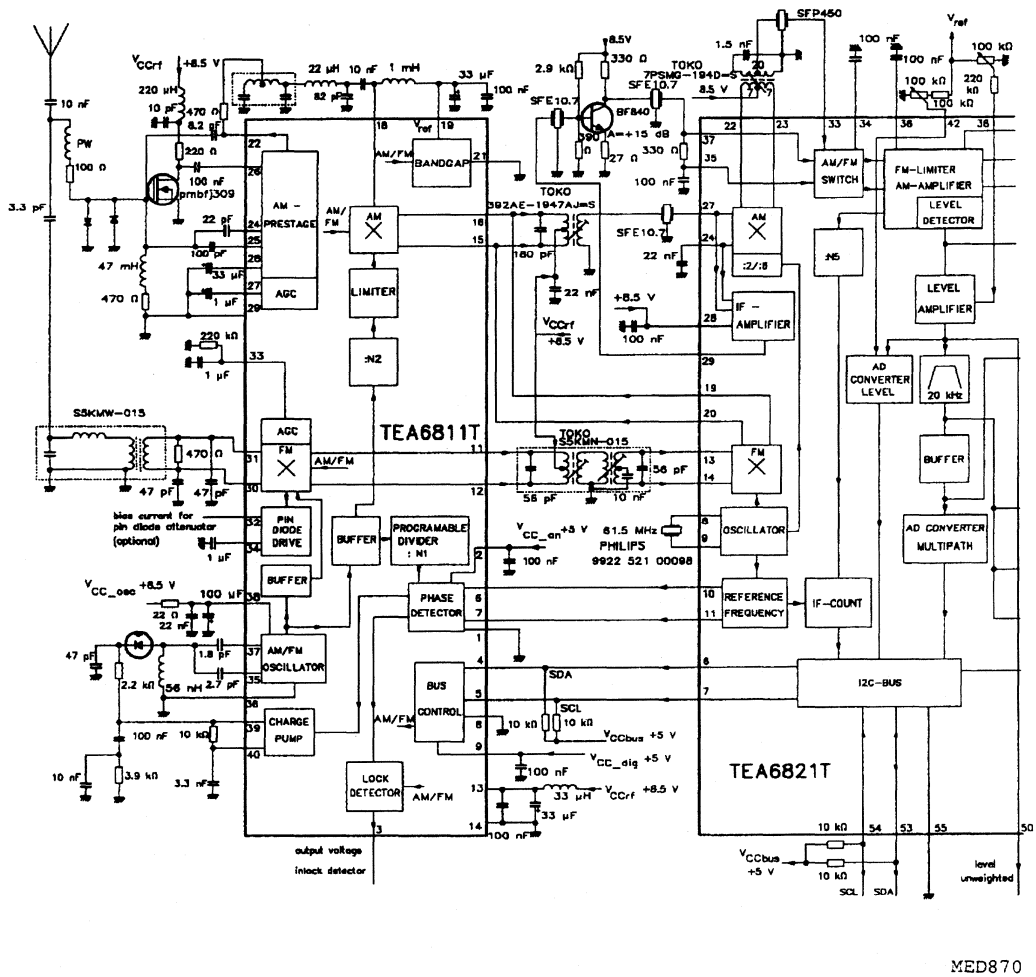


Fig.3 ICE91 application diagram (continued in Fig.4).

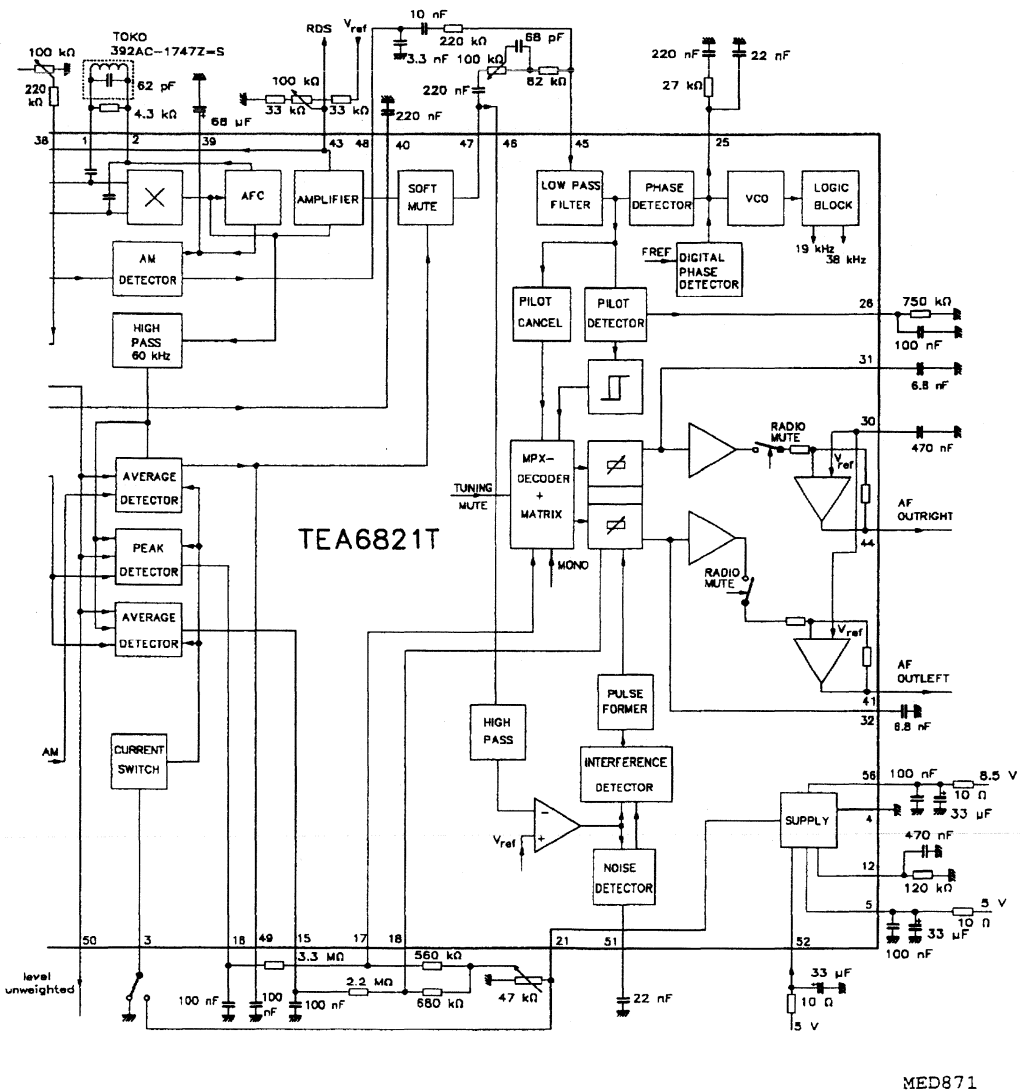


Fig.4 ICE91 application diagram (continued from Fig.3).

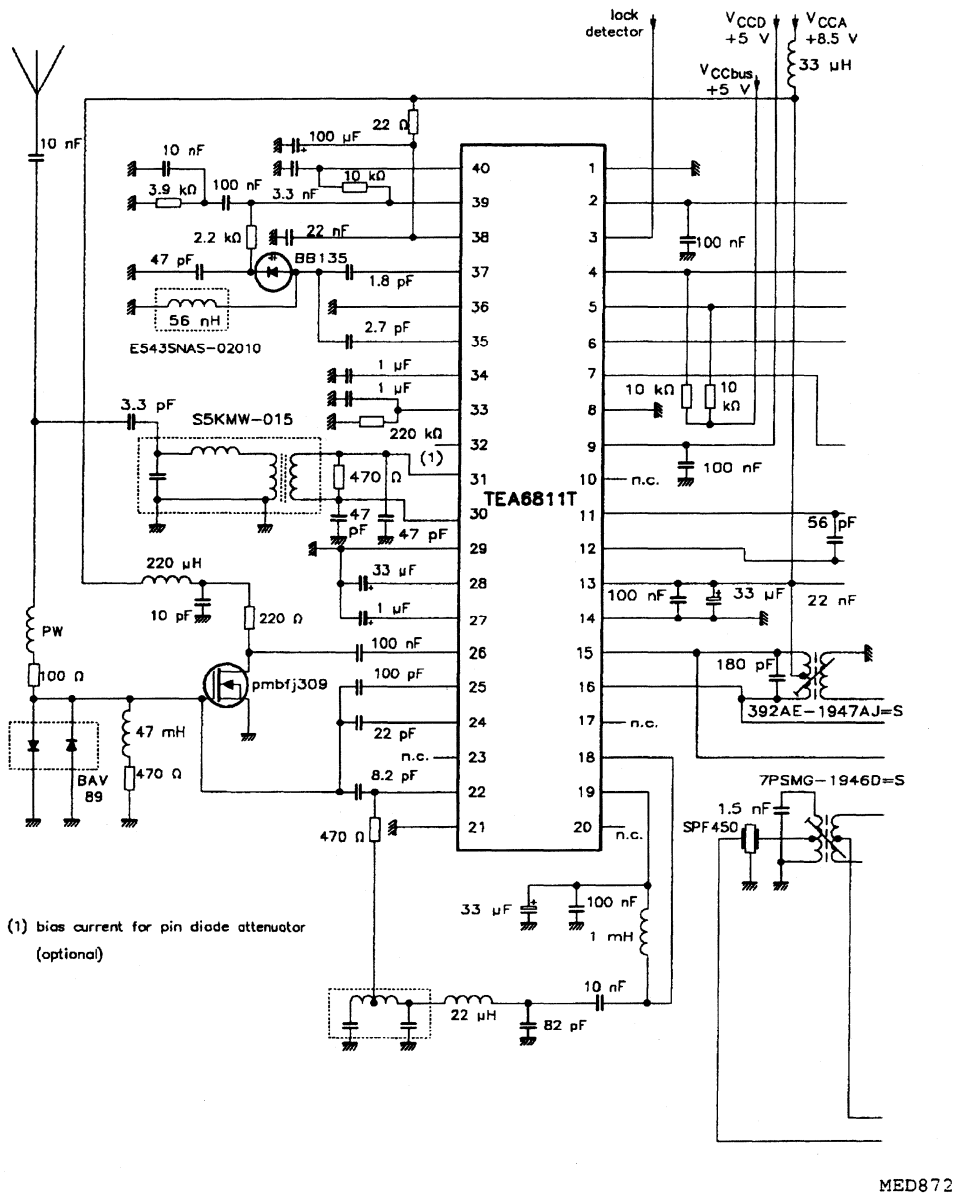


Fig.5 AM/FM car radio receiver with TEA6811T and TEA6821T (continued in Fig.6).

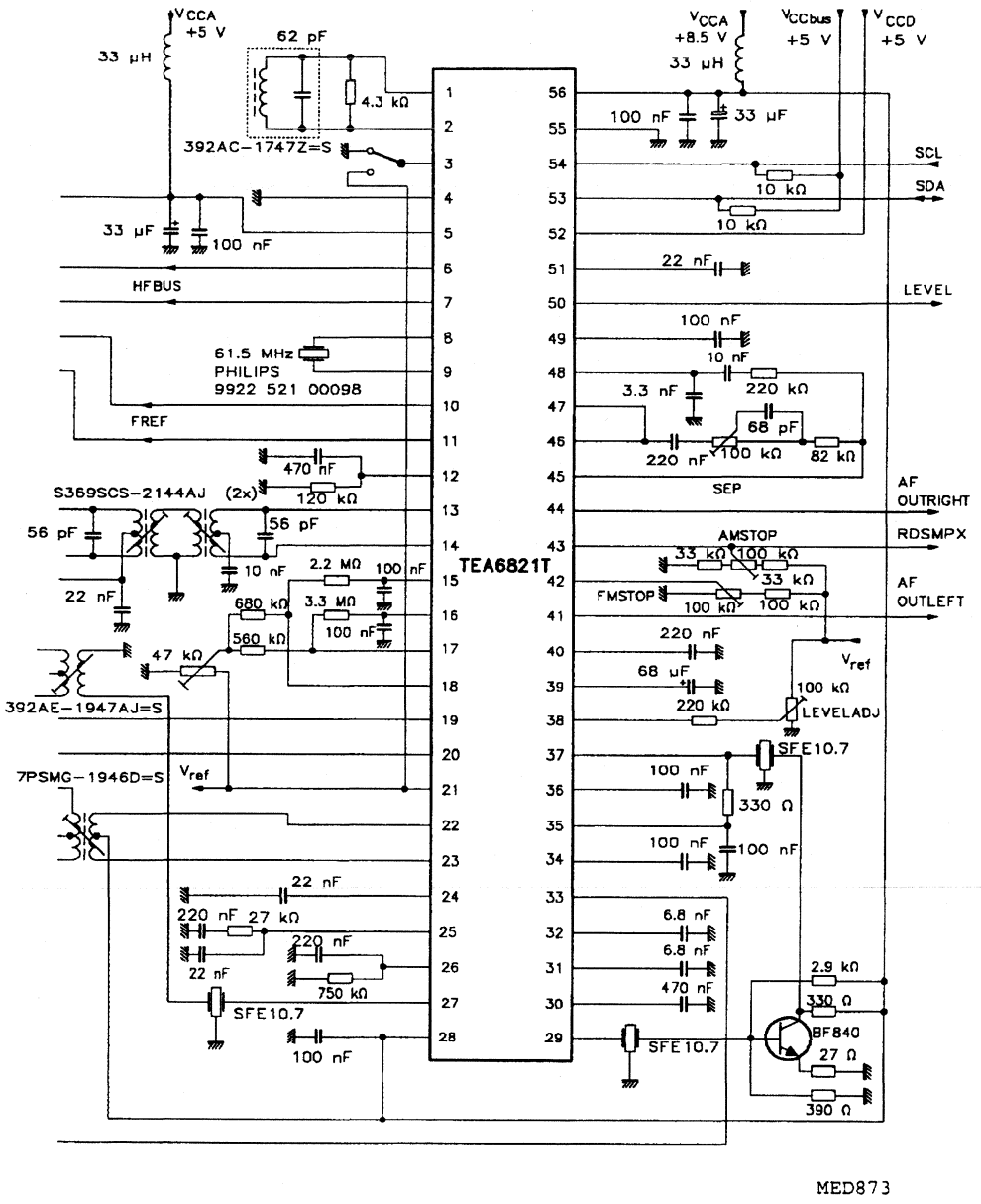


Fig.6 AM/FM car radio receiver with TEA6811T and TEA6821T (continued from Fig.5).

PINNING

SYMBOL	PIN	DESCRIPTION
QDET1	1	demodulator tank
QDET2	2	demodulator tank
TSWITCH	3	time switch
GND	4	analog ground
V_{P5}	5	5 V supply voltage
HFBUS1	6	HF bus, pull-up to 5 V
HFBUS2	7	HF bus, pull-up to 5 V
XTAL1	8	crystal oscillator
XTAL2	9	crystal oscillator
F_{REFP}	10	PLL reference frequency
F_{REFN}	11	PLL reference frequency
I_{REF}	12	reference current
FMIF1IN1	13	70 MHz FM-IF input
FMIF1IN2	14	70 MHz FM-IF input
TSDR	15	time constant for SDR
TSDS	16	time constant for SDS
V_{SDS}	17	SDS control voltage
V_{SDR}	18	SDR control voltage
FMIF2OUT1	19	FM mixer output
FMIF2OUT2	20	FM mixer output
V_{REF}	21	reference voltage
AMIF2OUT1	22	AM mixer output
AMIF2OUT2	23	AM mixer output
FMAMDEC	24	FM/AM 10.7 MHz decoupling
PHASEDET	25	phase detector
PILDET	26	pilot detector
FMAM10.7	27	FM/AM 10.7 MHz input
V_{PIF}	28	V_P IF amplifier

SYMBOL	PIN	DESCRIPTION
FMIFAMPOUT	29	FM-IF amplifier output
AFGND	30	AF ground
DEEMPHR	31	de-emphasis capacitor right
DEEMPHL	32	de-emphasis capacitor left
AMIF2IN1	33	AM IF2 input 1
AMIF2IN2	34	AM IF2 input 2
FMIN2	35	FM limiter input
DCFEED	36	DC feed FM limiter
FMIN1	37	FM limiter input
LEVELADJ	38	level adjust
C_{AFC}	39	AFC capacitor
MPBUF	40	multipath buffer time constant
OUTLEFT	41	AF output left
FMSTOP	42	FMSTOP adjust
RDS/AMSTOP	43	MPX for RDS/AMSTOP adjust
OUTRIGHT	44	AF output right
MPXIN	45	stereo decoder MPX input
IAC_{IN}	46	IAC input
MPXOUT	47	FM demodulator MPX output
AMAFOUT	48	AM demodulator AF output
V_{MUTAML}	49	mute voltage / AM level
LEVELUNWEIG	50	level unweighted
$I_{ACCONTR}$	51	IAC control voltage
V_{PDIG}	52	V_P digital
SDA	53	SDA, pull-up to 5 V
SCL	54	SCL, pull-up to 5 V
BUSGND	55	bus ground
$V_{P8.5}$	56	V_P 8.5 V

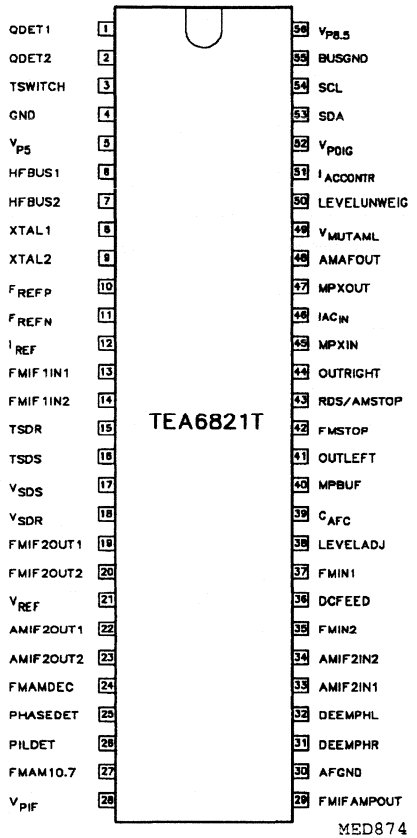


Fig.7 Pin configuration.

In Car Entertainment (ICE) car radio TEA6822T

FEATURES

General

- FM mixer for conversion from FM-IF1 = 72.2 MHz to FM-IF2 = 10.7 MHz
- AM mixer for conversion from AM-IF1 = 10.7 MHz to AM-IF2 = 450 kHz
- FM-IF gain stage
- Crystal oscillator providing mixer frequencies and references for IF-count and stereo decoder
- FM quadrature demodulator with automatic centre frequency adjustment and THD compensation
- Level, multi-path and noise detectors
- Soft mute
- Stereo noise cancelling and variable de-emphasis
- PLL stereo decoder
- Noise blanker
- AM IF-amplifier and demodulator
- I²C-bus transceiver with interface to enable direct data transfer to radio front-end
- IF-count for AM and FM
- Reference frequency generation for PLL synthesizer.

Stereo decoder

- Adjustment-free PLL-VCO
- Pilot depending mono/stereo switching
- Analog control of mono/stereo blend
- Adjacent channel noise suppression (114 kHz)
- Pilot cancelled
- Analog control of de-emphasis
- Integrated low-pass filters for 190 kHz adjacent channel interferences and signal delay for interference absorption circuit.

GENERAL DESCRIPTION

The TEA6822T together with the TEA6810T/TEA6811T forms an AM/FM electronic tuned car radio in a double conversion receiver concept.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6822T	VSO56	plastic very small outline package; 56 leads	SOT190-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA1}	analog supply voltage 1 (+5 V; pin 5)	note 1	4.5	5.0	5.5	V
		operating range	4.75	5.0	5.25	V
I_{DDA1}	analog supply current 1 (pin 5)	FM mode	18	21	25	mA
		AM mode	14	17	21	mA
$I_{19} + I_{20}$	total FM mixer output current		4.8	6.0	7.2	mA
$I_{22} + I_{23}$	total AM mixer output current		10	12	14	mA
V_{DDA2}	analog supply voltage 2 (pin 28)	note 1	7	8.5	10	V
		operating range	8.1	8.5	8.9	V
I_{DDA2}	analog supply current 2 (pin 28)	FM mode	2.4	3.0	3.6	mA
V_{DDA3}	analog supply voltage 3 (+8.5 V; pin 56)	note 1	7	8.5	10	V
		operating range	8.1	8.5	8.9	V
I_{DDA3}	analog supply current 3 (pin 56)	FM mode	19	24	28	mA
		AM mode	9.5	12	15	mA
V_{DDD}	digital supply voltage 1 (+5 V; pin 5)	note 1	4.5	5.0	5.5	V
		operating range	4.75	5.0	5.25	V
I_{DDD}	digital supply current (pin 52)	note 1	8	10	12	mA
$\frac{S+N}{N}$	signal-plus-noise-to-noise ratio	ΔFM mode; f = 22.5 kHz at pins 43 and 47	66	75	–	dB
		AM mode; m = 0.3	54	60	–	dB
THD	total harmonic distortion	FM mode; Δf = 75 kHz	–	0.1	0.35	%
		AM mode	–	1.5	3	%
α_{cs}	channel separation (adjusted)		40	–	–	dB
T_{amb}	operating ambient temperature		−40	–	+85	°C

Note

1. IC is operating; specified parameters may deviate from limits which are valid for operating range.

BLOCK DIAGRAM

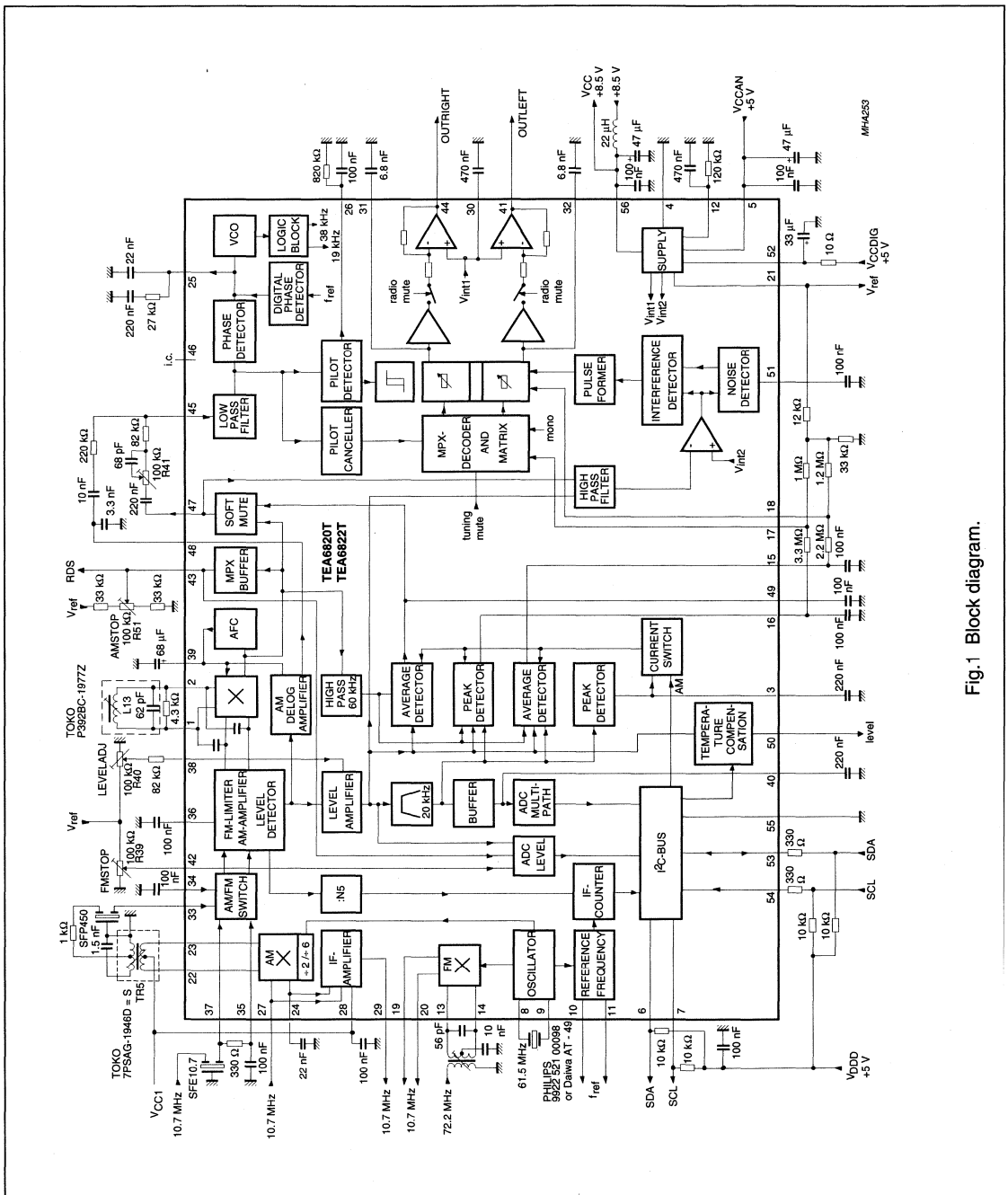


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
QDET1	1	demodulator tank 1
QDET2	2	demodulator tank 2
TSWITCH	3	time switch
AGND	4	analog ground
V_{DDA1}	5	analog supply voltage 1 (+5 V)
HFBUS1	6	HF bus 1; pull-up to 5 V
HFBUS2	7	HF bus 2; pull-up to 5 V
XTAL1	8	crystal oscillator 1
XTAL2	9	crystal oscillator 2
f_{ref1}	10	PLL reference output frequency 1
f_{ref2}	11	PLL reference output frequency 2
I_{ref}	12	reference current
FMIF1IN1	13	72 MHz FM-IF input 1
FMIF1IN2	14	72 MHz FM-IF input 2
TSDR	15	time constant for SDR
TSDS	16	time constant for SDS
V_{SDS}	17	SDS control voltage
V_{SDR}	18	SDR control voltage
FMIF2OUT1	19	FM mixer output 1
FMIF2OUT2	20	FM mixer output 2
V_{ref}	21	reference voltage
AMIF2OUT1	22	AM mixer output 1
AMIF2OUT2	23	AM mixer output 2
FMAMDEC	24	FM/AM 10.7 MHz decoupling
PHASEDET	25	phase detector
PILDET	26	pilot detector
FMAM10.7	27	FM/AM 10.7 MHz input
V_{DDA2}	28	analog supply voltage 2

SYMBOL	PIN	DESCRIPTION
FMIFAMPOUT	29	FM-IF amplifier output
AFGND	30	AF ground
DEEMPHR	31	de-emphasis capacitor right
DEEMPHL	32	de-emphasis capacitor left
AMIF2IN1	33	AM-IF2 input 1
AMIF2IN2	34	AM-IF2 input 2
FMIN2	35	FM limiter input
DCFEED	36	DC feed FM limiter
FMIN1	37	FM limiter input
LEVELADJ	38	level adjustment
C_{AFC}	39	AFC capacitor
MPBUF	40	multi-path buffer time constant
OUTLEFT	41	AF output left
FMSTOP	42	FMSTOP adjustment
RDS/AMSTOP	43	MPX for RDS/AMSTOP adjustment
OUTRIGHT	44	AF output right
MPXIN	45	stereo decoder MPX input
i.c.	46	internally connected
MPXOUT	47	FM demodulator MPX output
AMAFOUT	48	AM demodulator AF output
$V_{mute/AML}$	49	mute voltage/AM level
LEVELUNWEIG	50	level unweighted
IAC_{CONTR}	51	IAC control voltage
V_{DDD}	52	digital supply voltage
SDA	53	SDA; pull-up to 5 V
SCL	54	SCL; pull-up to 5 V
DGND	55	digital ground
V_{DDA3}	56	analog supply voltage 3 (8.5 V)

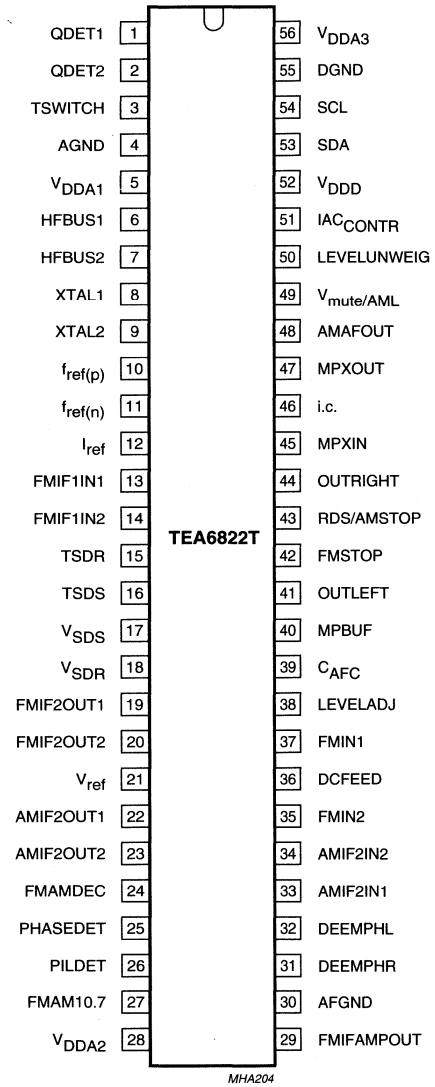


Fig.2 Pin configuration.

In Car Entertainment (ICE) car radio TEA6824T

FEATURES

- FM mixer for conversion from FM-IF_1 = 72.2 MHz to FM-IF_2 = 10.7 MHz
- AM mixer for conversion from AM-IF_1 = 10.7 MHz to AM-IF_2 = 450 kHz
- FM-IF gain stage
- Crystal oscillator providing mixer frequencies and references for IF-counter
- FM quadrature demodulator with automatic centre frequency adjustment and THD compensation
- AM-IF-amplifier and demodulator
- I^2C-bus transceiver with interface to enable direct data transfer to radio front-end
- IF-count for AM and FM
- Analog-to-digital conversion of level voltage and multi-path information
- Reference frequency generation for PLL synthesizer.

GENERAL DESCRIPTION

The TEA6824T together with the TEA6810T forms the receiver part of an AM/FM electronically tuned car radio providing FM MPX signal and AM AF signal for Car Digital Signal Processor (CDSP) applications.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6824T	VSO56	plastic very small outline package; 56 leads; face down	SOT190-2

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA1}	analog supply voltage 1 (+5 V; pin 5)	note 1	4.5	5.0	5.5	V
		operating range	4.75	5.0	5.25	V
I_{DDA1}	analog supply current 1 (pin 5)	FM mode	17	21	25	mA
		AM mode	14	17	21	mA
$I_{19} + I_{20}$	total FM mixer output current (pins 19 and 20)		4.8	6.0	7.2	mA
$I_{22} + I_{23}$	total AM mixer output current (pins 22 and 23)		10	12	14	mA
V_{DDA2}	analog supply voltage 2 (pin 28)	note 1	7.0	8.5	10	V
		operating range	8.1	8.5	8.9	V
I_{DDA2}	analog supply current 2 (pin 28)	FM mode	2.4	3.0	3.6	mA
V_{DDA3}	analog supply voltage 3 (+8.5 V; pin 56)	note 1	7.0	8.5	10	V
		operating range	8.1	8.5	8.9	V
I_{DDA3}	analog supply current 3 (pin 56)	FM mode	19	25	31	mA
		AM mode	9.5	12	15	mA
V_{DDD}	digital supply voltage 1 (+5 V; pin 5)	note 1	4.5	5.0	5.5	V
		operating range	4.75	5.0	5.25	V
I_{DDD}	digital supply current (pin 52)	note 1	8	10	12	mA
$\frac{S+N}{N}$	signal plus noise-to-noise ratio	FM mode; Δf = 22.5 kHz at pin 47	66	75	–	dB
		AM mode; m = 0.3	54	60	–	dB
THD	total harmonic distortion	FM mode; Δf = 75 kHz	–	0.1	0.35	%
		AM mode	–	1.5	3.0	%
T_{amb}	operating ambient temperature		−40	–	+85	°C

Note

1. IC is operating; specified parameters may deviate from limits which are valid for operating range.

BLOCK DIAGRAM

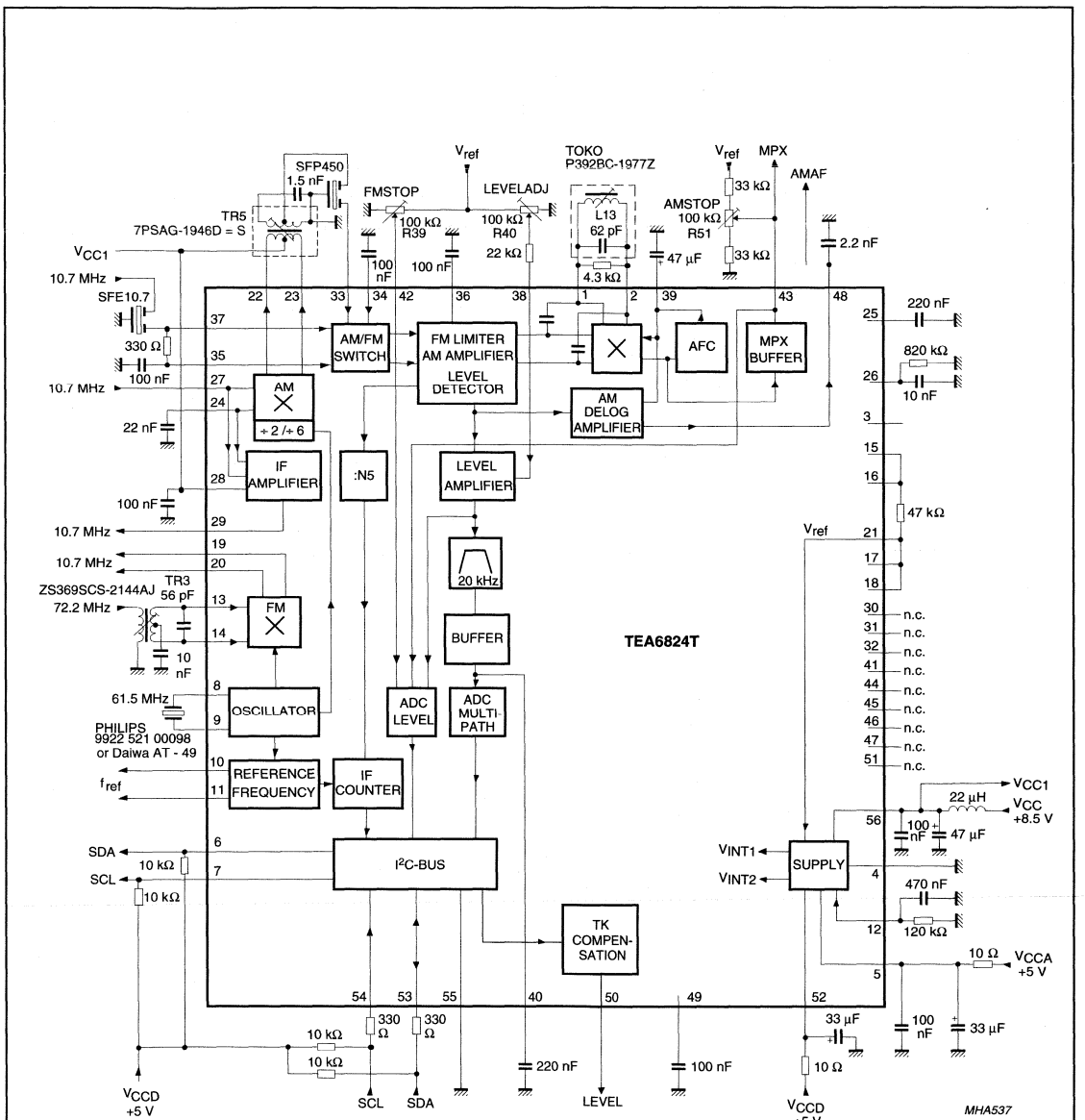


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
QDET1	1	demodulator tank 1
QDET2	2	demodulator tank 2
REFIN1	3	reference input 1
AGND	4	analog ground
V_{DDA1}	5	analog supply voltage 1 (+5 V)
HFBUS1	6	HF bus 1 output; pull-up to +5 V
HFBUS2	7	HF bus 2 output; pull-up to +5 V
XTAL1	8	crystal oscillator 1
XTAL2	9	crystal oscillator 2
$f_{ref(p)}$	10	PLL reference frequency output p
$f_{ref(n)}$	11	PLL reference frequency output n
I_{ref}	12	reference current input
FMIF1IN1	13	72 MHz FM-IF input 1
FMIF1IN2	14	72 MHz FM-IF input 2
REFIN2	15	reference input 2
REFIN3	16	reference input 3
REFIN4	17	reference input 4
REFIN5	18	reference input 5
FMIF2OUT1	19	FM mixer output 1
FMIF2OUT2	20	FM mixer output 2
V_{ref}	21	reference voltage input
AMIF2OUT1	22	AM mixer output 1
AMIF2OUT2	23	AM mixer output 2
FMAMDEC	24	FM/AM 10.7 MHz decoupling input
DEC1	25	decoupling 1
DEC2	26	decoupling 2
FMAM10.7	27	FM/AM 10.7 MHz input
V_{DDA2}	28	analog supply voltage 2

SYMBOL	PIN	DESCRIPTION
FMIFAMPOUT	29	FM-IF-amplifier output
n.c.	30	not connected
n.c.	31	not connected
n.c.	32	not connected
AMIF2IN1	33	AM-IF_2 input 1
AMIF2IN2	34	AM-IF_2 input 2
FMIN2	35	FM limiter input 2
DCFEED	36	DC feed FM limiter
FMIN1	37	FM limiter input 1
LEVELADJ	38	level adjustment
C_{AFC}	39	AFC capacitor
MPBUF	40	multi-path buffer time constant
n.c.	41	not connected
FMSTOP	42	FMSTOP adjustment
MPXOUT	43	FM demodulator MPX output
n.c.	44	not connected
n.c.	45	not connected
n.c.	46	not connected
n.c.	47	not connected
AMAFOUT	48	AM demodulator AF output
DEC3	49	decoupling 3
LEVELUNWEIG	50	level unweighted output
n.c.	51	not connected
V_{DDD}	52	digital supply voltage (+5 V)
SDA	53	serial data input/output; pull-up to +5 V; I^2C-bus
SCL	54	serial clock input; pull-up to +5 V; I^2C-bus
DGND	55	digital ground
V_{DDA3}	56	analog supply voltage 3 (+8.5 V)

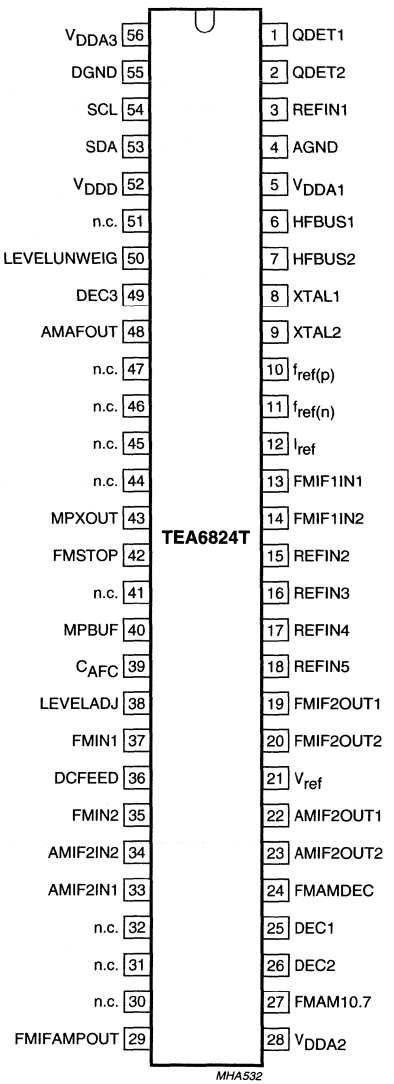


Fig.2 Pin configuration.

Data amplifier and laser supply circuit for CD and read-only optical systems (HDALAS)

TZA1015

FEATURES

- Six input buffer amplifiers with low-pass filtering and virtually no offset
- Universal photodiode IC interface using internal conversion resistors
- RF data amplifier with wide bandwidth designed for data rates up to a maximum of 30×
- Programmable RF gain for CD-A/V, CD-R, CD-R/W and CD-ROM applications
- Programmable RF bandwidth for optimal playability
- Radial error signal for fast track counting
- Programmable RF/Fast Track Count (FTC) gain for optimal dynamic range
- Fully automatic laser control including stabilization and on/off switch plus a separate supply for power efficiency
- Automatic monitor diode polarity selection
- Adjustable laser bandwidth and laser switch-on current slope using external capacitor
- Protection circuit to prevent laser damage due to supply voltage dip
- Optimized interconnection between data amplifier and Philips' digital signal processor family (CD7, ACE and MACE)
- Wide supply voltage range
- Wide temperature range
- Low power consumption.

GENERAL DESCRIPTION

The TZA1015 is a data amplifier and laser supply circuit for 3-beam pick-up detectors found in a wide range of CD and read-only optical systems.

The device contains 6 transimpedance amplifiers to amplify and filter the focus and radial photo diode voltage input signals. The preamplifier forms a versatile, programmable interface from voltage output CD mechanisms to the Philips' digital signal processor family.

The dynamic range of this preamplifier/processor combination can be optimized for the LF servo and RF data paths. The servo channel gain is set by the ADC range of the processor. The RF data channel can be programmed in the TZA1015 preamplifier.
The programmable RF bandwidth allows this device to be used in CD-A/V applications or CD-R, CD-R/W and CD-ROM applications with a data rate up to a maximum of 30×. The RF and LF gain can be adapted for CD-A/V, CD-R and CD-ROM discs or CD-R/W discs by means of a gain switch. In addition to this gain switch the RF gain is programmable to guarantee optimal playability. In order to enable minimal access time the TZA1015 generates a Fast Track Count signal which enables the decoder (ACE or MACE) to count the number of tracks during a track jump.

The device can accommodate astigmatic, single Foucault and double Foucault detectors and can be used with all laser and N- or P-sub monitor diodes. The Automatic Power Control circuit (APC) will maintain control over the laser diode current. With an on-chip reference voltage generator, a constant and stabilized output power is ensured independent of ageing. A separate power supply connection allows the internal power dissipation to be reduced by connecting a low voltage supply.

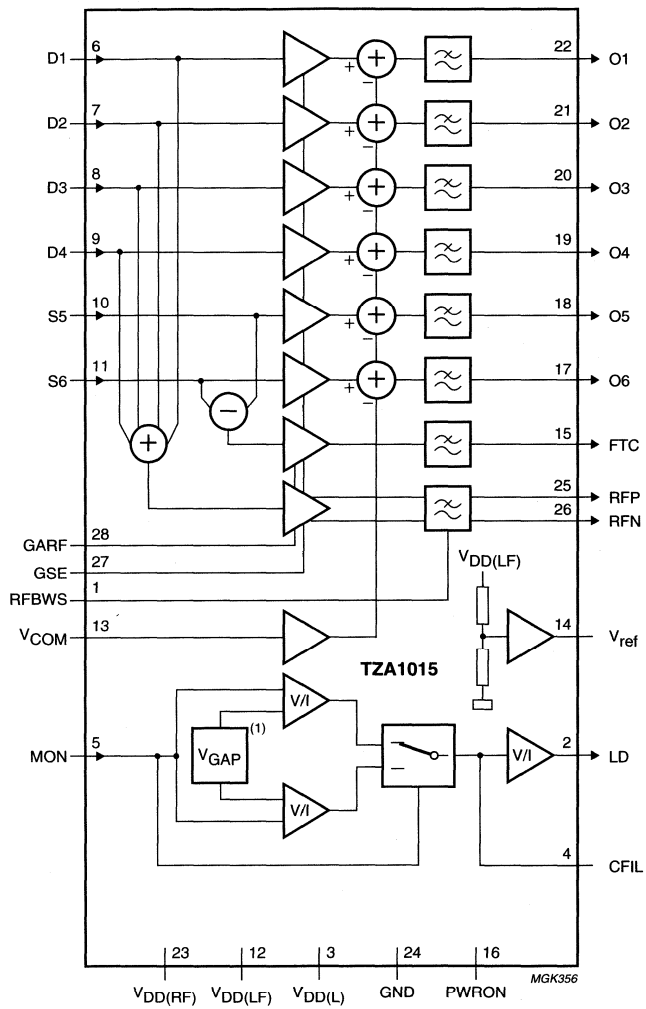
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA1015T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$V_{DD(RF,LF)}$	supply voltage		4.5	5.0	5.5	V
$V_{DD(LASER)}$	laser supply voltage		3	–	5.5	V
LF amplifiers						
I_{OS}	channel matching		–	–	1	%FS
$B_{(-3\ dB)}$	–3 dB bandwidth		65	90	115	kHz
RF amplifier						
$B_{(-3\ dB)}$	–3 dB bandwidth	programmable; GARF = open-circuit	7.5	10	12.5	MHz
			15	20	25	MHz
			37	50	63	MHz
$t_{d(f)(RF)}$	RF flatness delay		–	–	0.4	ns
Laser supply						
$I_{o(LASER)(min)}$	minimum laser output current	$V_{DD(LASER)}$ = 3 V	–	–	100	mA
$V_{i(mon)}$	monitor input voltage					
	N-type monitor		–	0.150	–	V
	P-type monitor		–	$V_{DD(RF,LF)}$ – 0.150	–	V
Temperature range						
T_{oper}	operating temperature		0	–	90	°C
T_{stg}	storage temperature		–65	–	+150	°C

BLOCK DIAGRAM



(1) Band-gap reference voltage.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
RFBWS	1	RF amplifier bandwidth select
LD	2	current output to the laser diode
$V_{DD(L)}$	3	laser supply voltage output
CFIL	4	external filter capacitor
MON	5	laser monitor diode input
D1	6	input photo diode amplifier 1 (central)
D2	7	input photo diode amplifier 2 (central)
D3	8	input photo diode amplifier 3 (central)
D4	9	input photo diode amplifier 4 (central)
S5	10	input photo diode amplifier 5 (satellite)
S6	11	input photo diode amplifier 6 (satellite)
$V_{DD(LF)}$	12	LF diode and FTC amplifier supply voltage
V_{COM}	13	common mode DC reference input
V_{ref}	14	DC reference voltage for biasing of Opto Electronic IC (OEIC)
FTC	15	fast track count amplifier output
PWRON	16	power on/off switch (V_{ref} bias generator always active)
O6	17	output photo diode amplifier 6
O5	18	output photo diode amplifier 5
O4	19	output photo diode amplifier 4
O3	20	output photo diode amplifier 3
O2	21	output photo diode amplifier 2
O1	22	output photo diode amplifier 1
$V_{DD(RF)}$	23	RF amplifier supply voltage
GND	24	ground
RFP	25	positive output RF data amplifier
RFN	26	negative output RF data amplifier
GSE	27	gain select for CD, CD-R, CD-R/W; RF and FTC amplifiers
GARF	28	gain adjust for RF and FTC amplifiers

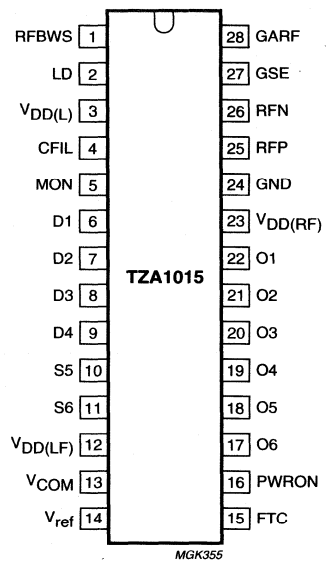
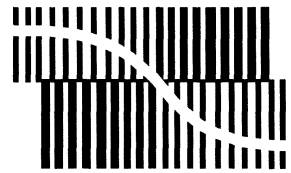


Fig.2 Pin configuration.

Low-power stereo bitstream ADC/DAC UDA1309H

FEATURES

- Low power
- Integrated high-pass filter to cancel DC offset (ADC)
- Analog loop-through function
- Multiple digital input/output formats possible
- $256f_s$ system clock frequency
- Several power-down modes
- Digital de-emphasis (DAC)
- Overload detector to enable automatic recording level adjustment (ADC)
- High dynamic range
- DAC requires only one capacitor for post-filtering
- Small 44-pin quad flat pack with 0.8 mm pitch
- $256f_s$ system clock frequency in Analog-to-Digital (AD) and Digital-to-Analog (DA) mode
- Choice of three system clock frequencies ($192f_s$, $256f_s$ or $384f_s$) in DA mode.



BITSTREAM CONVERSION

APPLICATION

- Portable digital audio equipment.

GENERAL DESCRIPTION

The UDA1309H is a single chip stereo analog-to-digital and digital-to-analog converter employing bitstream conversion techniques. The device is eminently suitable for use in low-power portable digital audio equipment which incorporates recording and playback functions.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1309H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

QUICK REFERENCE DATA

$V_{DDD} = V_{DDA} = V_{DDO} = V_{DDD(F)} = 5$ V; $V_{SSD} = V_{SSA} = V_{SSO} = V_{SSD(F)} = 0$ V; $T_{amb} = 25$ °C; full scale sine wave input; mode 1; $f_i = 1$ kHz; 16-bit input data; conversion rate = 44.1 kHz; measurement bandwidth = 10 Hz to 20 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$V_{DDA(AD)}$	ADC analog supply voltage (pin 8)		4.5	5.0	5.5	V
$V_{DDA(DA)}$	DAC analog supply voltage (pin 25)		4.5	5.0	5.5	V
V_{DDO}	operational amplifiers supply voltage (pin 19)		4.5	5.0	5.5	V
V_{DDD}	ADC and DAC digital supply voltage (pin 28)		4.5	5.0	5.5	V
$V_{DDD(F)}$	digital filters supply voltage (pin 34)		4.5	5.0	5.5	V
$I_{DDA(AD)}$	ADC analog supply current (pin 8)		–	9	13.5	mA
$I_{DDA(DA)}$	DAC analog supply current (pin 25)		–	4.5	6.8	mA
I_{DDO}	operational amplifiers supply current (pin 19)		–	14	21	mA
I_{DDD}	ADC and DAC digital supply current (pin 28)		–	0.2	0.5	mA
$I_{DDD(F)}$	digital filters supply current (pin 34)		–	24	36	mA
T_{amb}	operating ambient temperature		–20	–	+75	°C
Analog-to-digital converter						
$V_{I(rms)}$	input voltage (RMS value)	note 1	0.9	1.0	1.1	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–85	tbf	dB
		at –60 dB; A-weighted	–	–35	–30	dB
S/N	idle channel signal-to-noise ratio	$V_I = 0$ V; A-weighted	tbf	95	–	dB
α_{cs}	channel separation		–	90	–	dB
Digital-to-analog converter						
$V_{O(rms)}$	output voltage (RMS value)	note 2	0.9	1.0	1.1	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–90	–82	dB
		at –60 dB; A-weighted	–	–38	–34	dB
		at –60 dB; A-weighted; note 3	–	–44	–	dB
S/N	idle channel signal-to-noise ratio	code 0000H; A-weighted	–	104	–	dB
α_{cs}	channel separation		90	100	–	dB

Notes

1. V_I for full scale digital output is a function of $V_{DDA(AD)}$ [1.0 V (RMS) at $V_{DDA(AD)} = 5.0$ V is equivalent to –1.0 dB in the digital domain].
2. At full scale digital input; no de-emphasis; $V_{O(rms)}$ is a function of $V_{DDA(DA)}$.
3. 18-bit input data.

BLOCK DIAGRAM

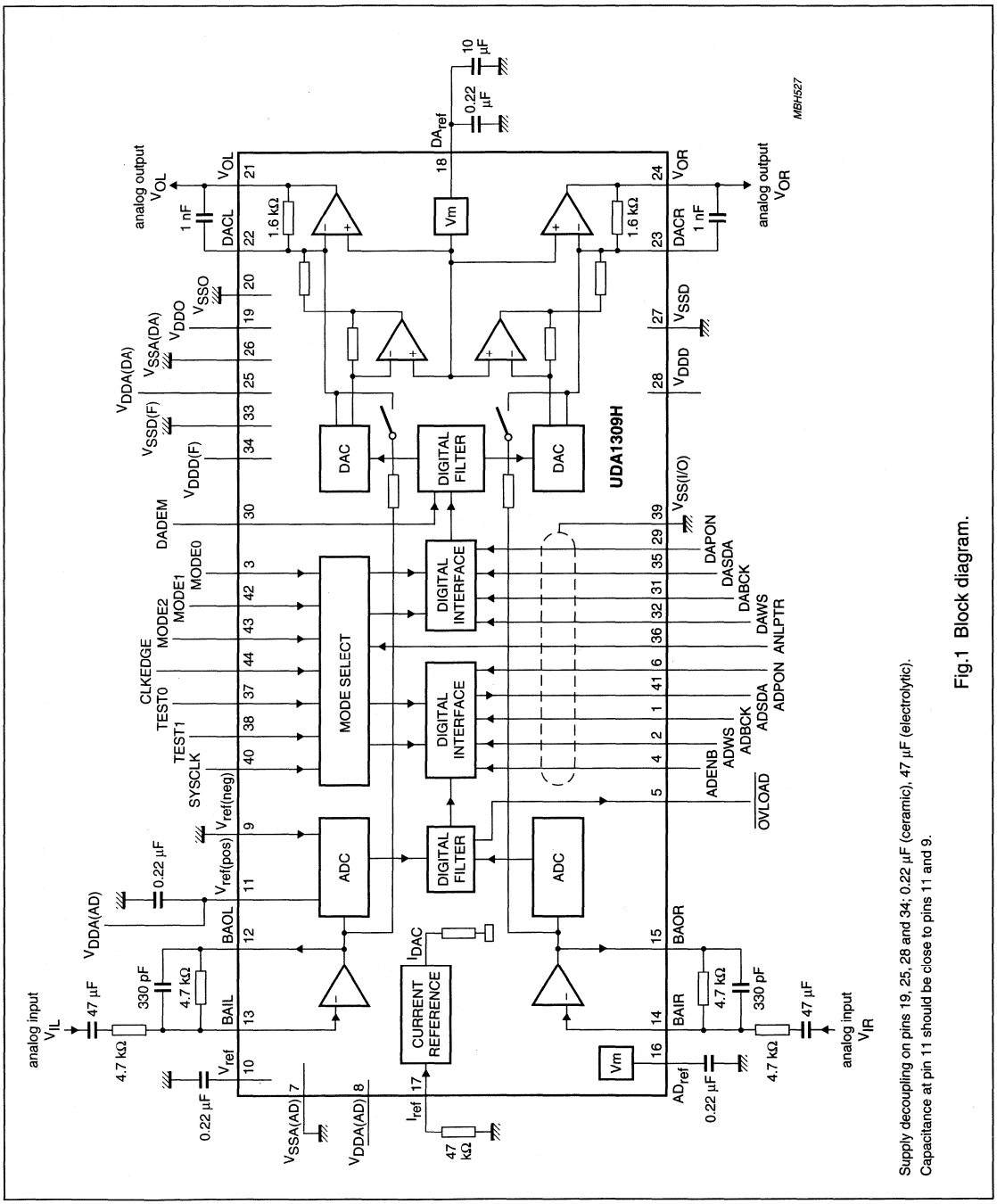


Fig.1 Block diagram.

Supply decoupling on pins 19, 25, 28 and 34; 0.22 µF (ceramic), 47 µF (electrolytic).
Capacitance at pin 11 should be close to pins 11 and 9.

PINNING

SYMBOL	PIN	DESCRIPTION
ADBCK	1	ADC input bit clock; $32f_s$ or $64f_s$
ADWS	2	ADC word select input at f_s
MODE0	3	ADC/DAC mode select input
ADENB	4	ADC serial data enable input (active HIGH)
$\overline{\text{OVLOAD}}$	5	ADC output overload flag (active LOW)
ADPON	6	ADC power-on-mode input (active HIGH)
$V_{SSA(AD)}$	7	ADC analog ground supply voltage
$V_{DDA(AD)}$	8	ADC analog supply voltage
$V_{ref(neg)}$	9	ADC negative reference voltage input (ground)
V_{ref}	10	ADC decoupling capacitor
$V_{ref(pos)}$	11	ADC positive reference voltage decoupling capacitor
BAOL	12	ADC input amplifier output left
BAIL	13	ADC input amplifier virtual ground left
BAIR	14	ADC input amplifier virtual ground right
BAOR	15	ADC input amplifier output right
AD_{ref}	16	ADC decoupling capacitor
I_{ref}	17	ADC/DAC reference current resistor input
DA_{ref}	18	DAC decoupling capacitor
V_{DDO}	19	ADC/DAC operational amplifier supply voltage
V_{SSO}	20	ADC/DAC operational amplifier ground supply voltage
V_{OL}	21	DAC output voltage left
DACL	22	DAC output current left
DACR	23	DAC output current right
V_{OR}	24	DAC output voltage right
$V_{DDA(DA)}$	25	DAC analog supply voltage
$V_{SSA(DA)}$	26	DAC analog ground supply voltage
V_{SSD}	27	ADC/DAC digital ground supply voltage
V_{DDD}	28	ADC/DAC digital supply voltage
DAPON	29	DAC power-on-mode input (active HIGH)
DADEM	30	DAC digital de-emphasis input (active HIGH)
DABCK	31	DAC input bit clock; $32f_s$, $48f_s$ or $64f_s$
DAWS	32	DAC word select input at f_s
$V_{SSD(F)}$	33	ADC/DAC digital filters ground supply voltage
$V_{DDD(F)}$	34	ADC/DAC digital filters supply voltage
DASDA	35	DAC serial data input
ANLPTR	36	ADC/DAC analog loop-through input (active HIGH)
TEST0	37	ADC/DAC enable test mode 0 input (LOW is normal mode)
TEST1	38	ADC/DAC enable test mode 1 input (LOW is normal mode)
$V_{SS(I/O)}$	39	ADC/DAC digital input/output ground supply voltage
SYSCLK	40	ADC/DAC system clock input ($f_{sys} = 256f_s$; DAC also $192f_s$ and $384f_s$)

SYMBOL	PIN	DESCRIPTION
ADSDA	41	ADC serial data output
MODE1	42	ADC/DAC mode 1 select input
MODE2	43	ADC/DAC mode 2 select input
CLKEDGE	44	ADC/DAC input bit clock rising/falling edge

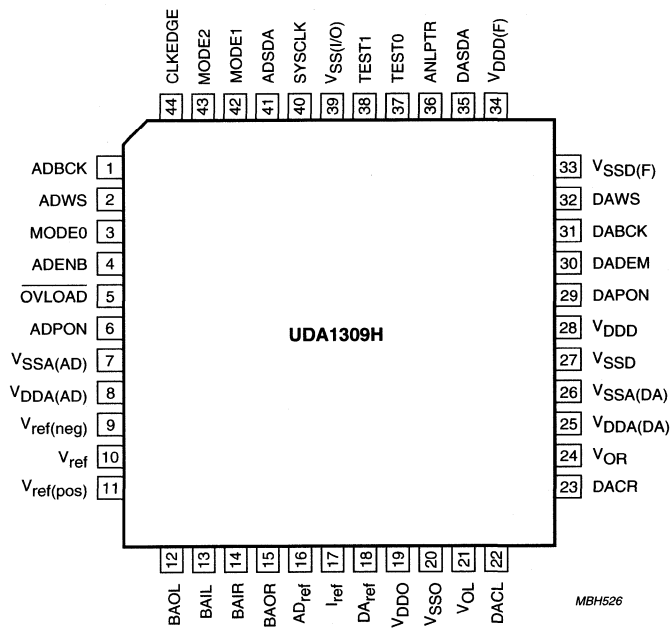


Fig.2 Pin configuration.

Universal Serial Bus (USB) Digital-to-Analog Converter (DAC)

UDA1321

FEATURES

General

- Complete stereo USB-DAC system with integrated filtering and line output drivers
- Supports USB-compliant audio multimedia devices over an industry standard USB-compatible 4-wire cable
- Supports 12 Mbits/s 'full speed' serial data transmission
- Fully automatic 'Plug-and-Play' operation
- Supports multiple audio data formats
- 3.3 V power supply
- Low power consumption
- Efficient power management mode
- On-chip master clock oscillator, only an external crystal is required
- High linearity
- Wide dynamic range
- Superior signal-to-noise ratio
- Low total harmonic distortion
- Easy application and inexpensive to implement
- Partly programmable USB descriptors via EEROM
- 28 lead Small Outline package (SO28) or 32 Shrink Dual Inline package (SDIP32).

Sound processing

- Separate digital volume control for left and right channel
- Soft mute
- Digital bass and treble tone control
- External Digital Sound Processor (DSP) option possible via standard I²S or Japanese digital I/O-format
- Selectable clipping prevention
- Selectable Dynamic Bass Boost (DBB)
- On-chip digital de-emphasis.

Document references

- *"USB Specification"*, release 1.0
- *"USB Device Class Definition for Audio Devices"*, release 0.9
- *"Device Class Definition for Human Interface Devices (HID)"*, release 1.0 draft 4
- *"USB HID Usage Table"*, release 0.7f.

GENERAL DESCRIPTION

The UDA1321 is a stereo CMOS digital-to-analog bitstream converter designed for USB-compliant audio devices and multimedia audio applications. The UDA1321 is an adaptive asynchronous sink USB audio device with a continuous sampling frequency range from 5 to 55 kHz. It contains a USB-interface, an embedded micro controller and an Asynchronous Digital-to-Analog Converter (ADAC).

The USB-interface is the interface between the USB, the ADAC and the microcontroller. The USB-interface consists of an analog front-end and a USB-processor. The analog front-end transforms the differential USB-data to a digital data stream. The USB-processor buffers incoming and outgoing data from the analog front-end and handles all low level USB protocols. The USB-processor selects the relevant data from the bus, performs an extensive error detection and separates control information (in- and out-going) and audio information (in-going only). The control information is made accessible to the microcontroller. The audio information becomes available at the digital I/O-output or is fed directly to the ADAC.

The microcontroller handles the high level USB protocols, translates the incoming control requests and takes care of the user interface, through general purpose pins, and an I²C port.

The ADAC enables the wide and continuous range of input sampling frequencies. By means of a Sample Frequency Generator (SFG), the ADAC is able to reconstruct the average sample frequency from the incoming audio samples. Furthermore the ADAC performs the sound processing. The ADAC consists of a FIFO, an unique audio feature processing DSP, the SFG, digital upsample filters, a variable hold register, a Noise Shaper (NS) and a Filter Stream DAC (FSDAC) with integrated filter and line output drivers. The audio information is applied to the ADAC via the USB-processor or via the digital I/O-input.

Via the digital I/O-bus an external DSP can be used for adding extra sound processing features.

The UDA1321 supports the standard I²S-bus data input format and the LSB justified serial data input format with word lengths of 16, 18 and 20 bits.

Universal Serial Bus (USB) Digital-to-Analog Converter (DAC)

UDA1321

The wide dynamic range of the bitstream conversion technique used in the UDA1321 guarantees a high audio sound quality.

APPLICATIONS

- USB monitors
- USB speakers
- USB headsets
- USB telephone/answering machines
- USB links in consumer audio devices.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power supplies						
V_{DD}	supply voltage	note 1	3.0	3.3	3.6	V
I_{DD}	supply current		–	50		mA
$I_{DD(ps)}$	supply current (power-saving mode)		–	18	–	mA
Dynamic performance DAC						
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	f_s = 44.1 kHz; R_L = 5 kΩ				
		at input signal of 1 kHz (0 dB)	–	–85	–80	dB
			–	0.0056	0.01	%
		at input signal of 1 kHz (–60 dB)	–	–30	–20	dB
			–	3.2	10.0	%
S/N	signal-to-noise ratio at bipolar zero	A-weighted at code 0000H	90	95	–	dBA
$V_{FS(o)(rms)}$	full-scale output voltage (RMS value)	V_{DD} = 3.3 V	–	0.66	–	V
General characteristics						
$f_{i(sample)}$	audio sample input frequency		5	–	55	kHz
T_{amb}	operating ambient temperature		0	25	70	°C

Note

1. All V_{DD} and V_{SS} pins must be connected to the same supply or ground respectively.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1321T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
UDA1321	SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1

BLOCK DIAGRAM

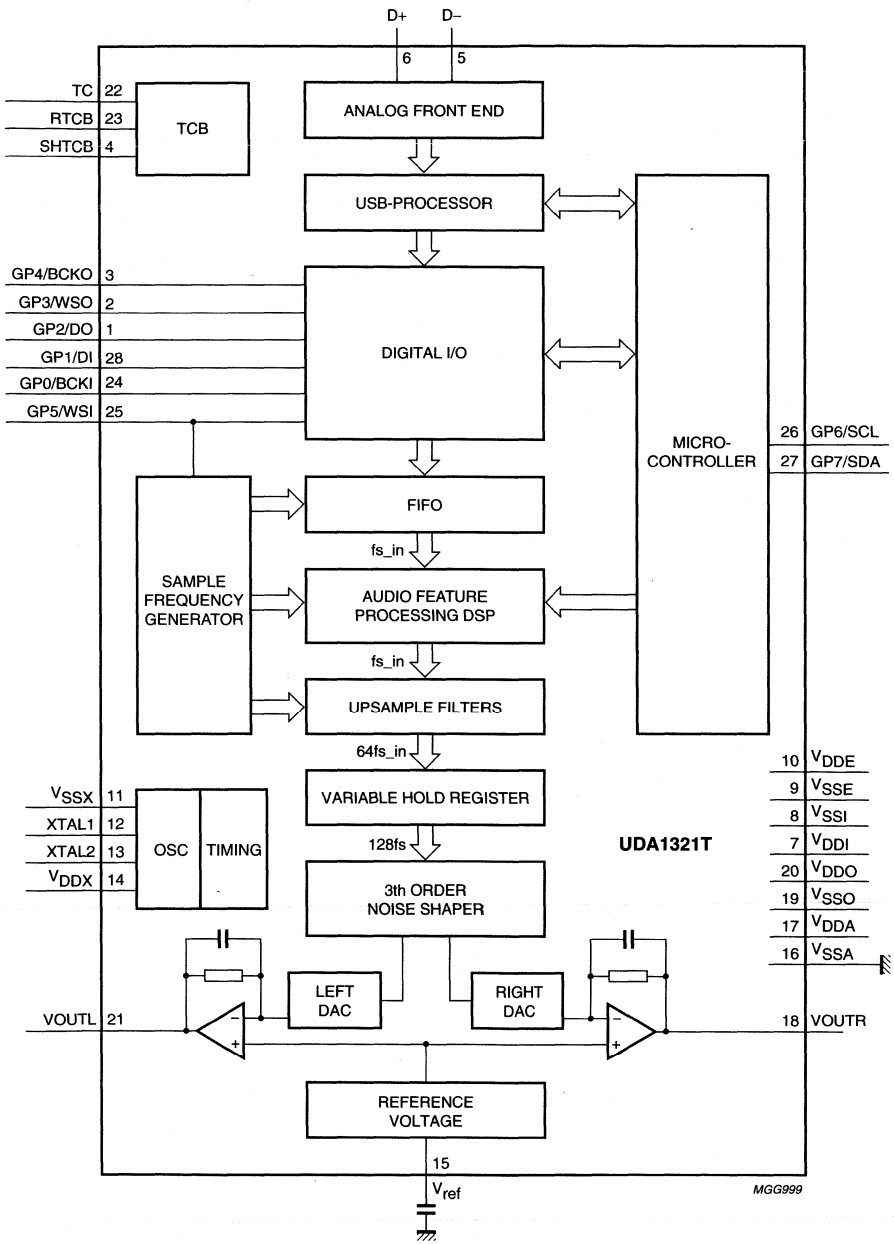


Fig.1 Block diagram SO28 pinning.

PINNING

SYMBOL	PIN SDIP32	PIN SO28	I/O	DESCRIPTION
GP2/DO	1	1	I/O	general purpose pin/data output pin for extra DSP chip (digital)
GP3/WSO	2	2	I/O	general purpose pin/master word select output pin for extra DSP chip (digital)
GP4/BCKO	3	3	I/O	general purpose pin/master bit clock output pin for extra DSP chip (digital)
SHTCB	4	4	I	shift clock TCB (active HIGH; digital)
	5		–	n.c.
D–	6	5	I/O	negative data line of the differential data bus conforming to the USB-standard (analog)
D+	7	6	I/O	positive data line of the differential data bus conforming to the USB-standard (analog)
V_{DDI}	8	7	–	digital supply digital core
V_{SSI}	9	8	–	digital ground core
V_{SSE}	10	9	–	digital ground I/O pads
V_{DDE}	11	10	–	digital supply I/O pads
	12		–	n.c.
V_{SSX}	13	11	–	crystal oscillator ground
XTAL1	14	12	I	crystal connection (analog)
XTAL2	15	13	O	crystal connection (analog)
V_{DDX}	16	14	–	supply crystal oscillator
	17		–	n.c.
V_{ref}	18	15	I	V_{ref} output pin (analog)
V_{SSA}	19	16	–	analog ground
V_{DDA}	20	17	–	analog supply
VOUTR	21	18	O	voltage output pin right channel (analog)
V_{SSO}	22	19	–	opamp ground
V_{DDO}	23	20	–	opamp supply
VOUTL	24	21	O	voltage output pin left channel (analog)
TC	25	22	I	test control pin (active HIGH; analog)
RTCB	26	23	I	asynchronous reset TCB (active HIGH; digital)
GP0/BCKI	27	24	I/O	general purpose pin (digital)
	28		–	n.c.
GP5/WSI	29	25	I/O	general purpose pin (digital)
GP6/SCL	30	26	I/O	general purpose pin/clock line I^2C-bus (digital)
GP7/SDA	31	27	I/O	general purpose pin/data line I^2C-bus (digital)
GP1/DI	32	28	I/O	general purpose pin/data input pin from extra DSP chip (digital)

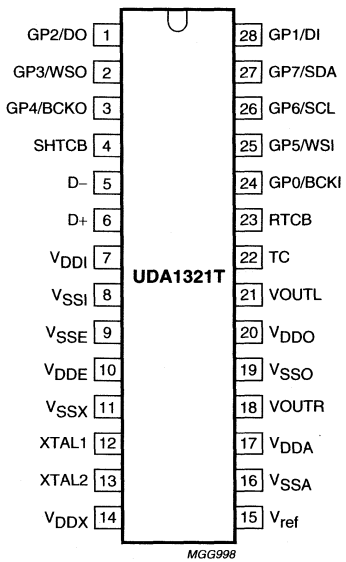


Fig.2 Pin configuration SO28.

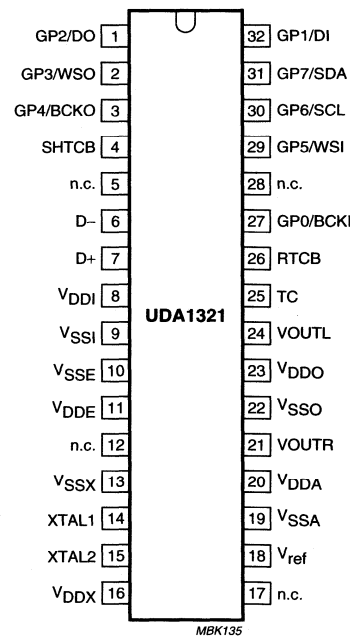


Fig.3 Pin configuration SDIP32.

Low-voltage low-power stereo audio CODEC with DSP features

UDA1340

FEATURES

General

- Low power consumption
- 3.0 V power supply
- 256, 384 and 512f_s system clock
- Small package size (SSOP28)
- ADC plus integrated high pass filter to cancel DC offset
- Overload detector for easy record level control
- Separate power control for ADC and DAC
- Integrated digital filter plus DAC
- No analog post filter required for DAC
- Easy application
- Functions controllable by microcontroller interface.

Multiple format input interface

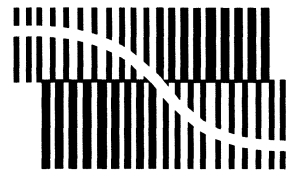
- I^2S-bus, MSB-justified and LSB-justified format compatible
- 1f_s input and output format data rate.

DAC digital sound processing

- Digital volume control
- Digital tone control, bass boost and treble
- dB-linear volume and tone control (low microcontroller load)
- Digital de-emphasis for 32, 44.1 and 48 kHz f_s
- Soft mute.

Advanced audio configuration

- Stereo single-ended input configuration
- Stereo line output (under microcontroller volume control)
- Power-down click prevention circuitry
- High linearity, dynamic range, low distortion.



BITSTREAM CONVERSION

GENERAL DESCRIPTION

The UDA1340 is a single-chip stereo Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) with signal processing features employing bitstream conversion techniques. The low power consumption and low voltage requirements make the device eminently suitable for use in low-voltage low-power portable digital audio equipment which incorporates recording and playback functions.

The UDA1340 supports the I^2S-bus data format with word lengths of up to 20 bits, the MSB-justified data format with word lengths of up to 20 bits and the LSB justified serial data format with word lengths of 16, 18 and 20 bits.

The UDA1340 has special sound processing features in playback mode, de-emphasis, volume, bass boost, treble, and soft mute, which can be controlled via the microcontroller interface.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1340M	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$V_{DDA(ADC)}$	ADC analog supply voltage		2.7	3.0	3.6	V
$V_{DDA(DAC)}$	DAC analog supply voltage		2.7	3.0	3.6	V
V_{DDO}	operational amplifiers supply voltage		2.7	3.0	3.6	V
V_{DDD}	digital supply voltage		2.7	3.0	3.6	V
$I_{DDA(ADC)}$	ADC supply current		–	4.5	–	mA
$I_{DDA(DAC)}$	DAC supply current		–	3.5	–	mA
I_{DDO}	operational amplifier supply current		–	4	–	mA
I_{DDD}	digital supply current		–	6	–	mA
$I_{PD(ADC)}$	digital ADC power-down supply current		–	3	–	mA
$I_{PD(DAC)}$	digital DAC power-down supply current		–	3	–	mA
T_{amb}	operating ambient temperature		−20	–	+85	°C
Analog-to-digital converter						
$V_{I(rms)}$	input voltage (RMS value)		–	0.8	–	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	−85	−80	dB
		at −60 dB; A-weighted	–	−35	−30	dBA
S/N	signal-to-noise ratio	V_i = 0 V; A-weighted	–	95	–	dBA
α_{cs}	channel separation		–	100	–	dB
Digital-to-analog converter						
$V_{o(rms)}$	output voltage (RMS value)		–	0.8	–	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	−85	−80	dB
		at −60 dB; A-weighted	–	−35	–	dBA
S/N	signal-to-noise ratio	code = 0; A weighted	–	100	–	dBA
α_{cs}	channel separation		–	100	–	dB
Power performance						
P_{ADDA}	power consumption in record and playback mode		–	54	–	mW
P_{DA}	power consumption in playback only mode		–	33	–	mW
P_{AD}	power consumption in record only mode		–	27	–	mW
P_{PD}	power consumption in power-down mode		–	6	–	mW

BLOCK DIAGRAM

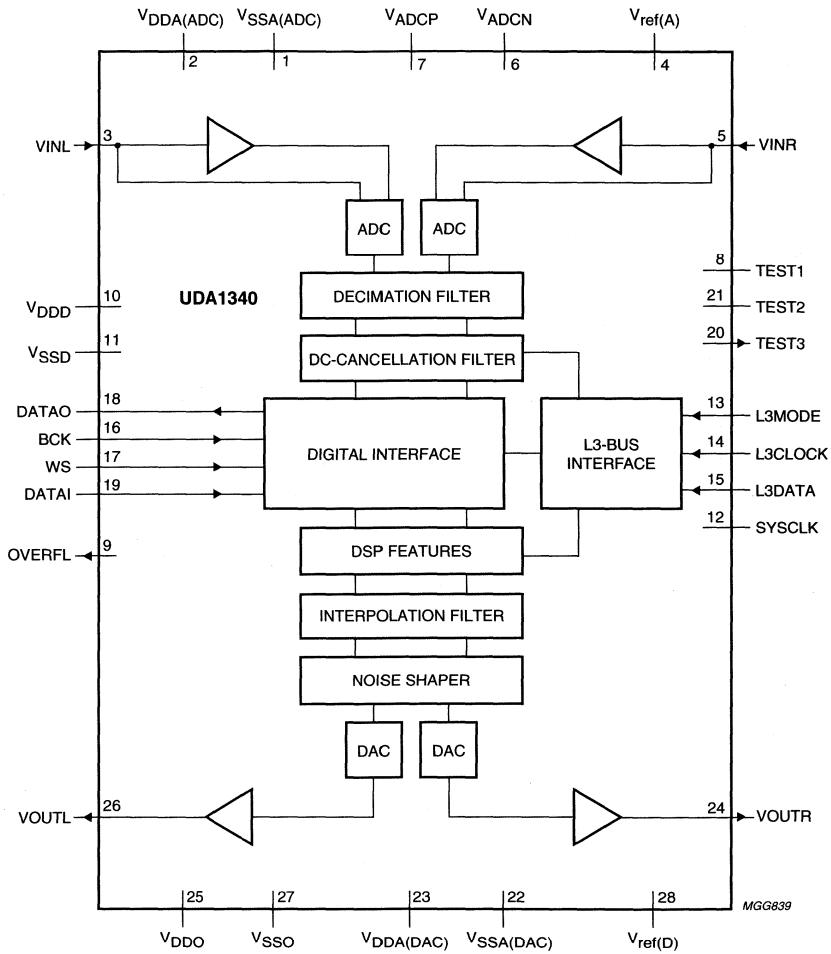


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	Description
$V_{SSA(ADC)}$	1	ADC analog ground
$V_{DDA(ADC)}$	2	ADC analog supply voltage
VINL	3	ADC input left
$V_{ref(A)}$	4	ADC reference voltage
VINR	5	ADC input right
V_{ADCN}	6	ADC negative reference voltage
V_{ADCP}	7	ADC positive reference voltage
TEST1	8	test control 1 (pull-down)
OVERFL	9	overload flag output
V_{DDD}	10	digital supply voltage
V_{SSD}	11	digital ground
SYSCLK	12	system clock 256, 384 or 512f_s
L3MODE	13	L3-bus mode input
L3CLOCK	14	L3-bus clock input
L3DATA	15	L3-bus data input
BCK	16	bit clock input
WS	17	word selection input
DATAO	18	data output
DATAI	19	data input
TEST3	20	test output
TEST2	21	test control 2 (pull-down)
$V_{SSA(DAC)}$	22	DAC analog ground
$V_{DDA(DAC)}$	23	DAC analog supply voltage
VOUTR	24	DAC output right
V_{DDO}	25	operational amplifier supply voltage
VOUTL	26	DAC output left
V_{SSO}	27	operational amplifier ground
$V_{ref(D)}$	28	DAC reference voltage

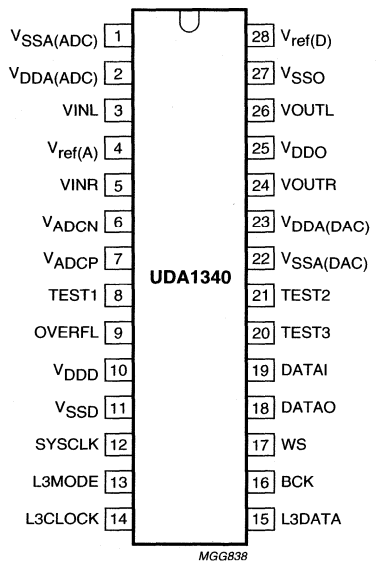


Fig.2 Pin configuration.

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Data handbook system

DATA HANDBOOK SYSTEM

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Printed in USA 517011/24M/03/312 Date of release: September 1997 Document order number: 9397 750 0245